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# Low power data converters for specific applications

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# Low power data converters for specific applications

by

Siamak Mortezapour

A dissertation submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering (Microelectronics)

Major Professor: Edward K.F. Lee

Iowa State University

Ames, Iowa

2000

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# ABSTRACT

Due to increasing importance of portable equipment and reduction of the supply voltage due to technology scaling, recent efforts in the design of mixed-signal circuits have focused on developing new techniques to reduce the power dissipation and supply voltage. Developing these new techniques requires research into new architectures and circuit techniques that enable both programmability and integration. Programmability allows each component to be used for different applications, reducing the total number of components, and increased integration by eliminating external components will reduce cost and power.

Since data converters are used in many different applications, in this thesis new low voltage and low power data converter techniques at both the architecture and circuit design levels are investigated to minimize power dissipation and supply voltage. To demonstrate the proposed techniques, test the performance of the proposed architectures, and verify their effectiveness in terms of power savings, five prototype chips are fabricated, tested, and presented.

First, a reconfigurable data converter (RDC) architecture is presented that can be programmed as an analog-to-digital converter (ADC), a digital-to-analog converter (DAC), or both. The reconfigurability of the RDC to different numbers of ADCs and

DACs having different speeds and resolutions makes it an ideal choice for analog test bus, mixed-mode boundary scan, and built-in self test applications.

Next, a new method for designing low power and small area ROMless direct digital frequency synthesizers (DDFSs) is presented. In this method, a non-linear digital-to-analog converter is used to replace the phase-to-sine amplitude ROM look-up table and the linear DAC in conventional DDFS. Since the non-linear DAC converts the phase information directly into analog sine wave, no phase-to-amplitude ROM look-up table is required.

Finally, a new low voltage technique based on biased inverting opamp that can have almost rail-to-rail voltage swing with continuously valid output is discussed. Based on this biasing technique, a 10-bit segmented R-2R DAC and an 8-bit successive approximation ADC are designed and presented.

# CHAPTER 1. INTRODUCTION

Consumer demand for low-power and low-voltage ICs has consistently grown because of the increasing importance of portable equipment and the reduction of the supply voltage due to technology scaling. Battery operated systems require low-voltage, low-power circuits. Sub-micron devices also require lower supply voltage. In this dissertation, several methods for designing low-power and low-voltage data converters for specific applications are introduced.

Many digital systems require several data converters to communicate with the outside world because most inputs and outputs are analog in nature. Nevertheless, not all of these data converters are used at the same time. For some applications, these converters will have different requirements. In this dissertation, an architecture that can be programmed as an analog-to-digital converter (ADC), a digital-to-analog converter (DAC), or both is presented. This reconfigurable data converter (RDC) can be used to trade off between speed, power and resolution [1]. One of the advantages of the RDC is the flexibility that it gives the user to choose ADC/DAC combinations for the desired application. Furthermore, this architecture enables the user to have DC and AC tests similar to the case of using analog test buses and analog boundary scan. In addition, it allows digitized analog signals to be observed and controlled via test

buses, similar to the mixed-mode boundary scan techniques. Therefore, it combines the advantages of both analog test buses and boundary scan techniques, while the area overhead of the proposed techniques is very low compared to the mixed-mode boundary scan techniques. This architecture can be potentially implemented inside a field programmable gate array (FPGA) to allow the FPGA to communicate with the analog world. It can also be used as a stand-alone product to give flexibility to the user to choose ADC/DAC combinations for the desired application. As for other pipelined data converters, fully digital error correction (self-calibration) can be applied to the RDC to improve its accuracy [2]. In order to demonstrate this concept, a prototype RDC design is presented and programmed as an 8-bit+ (8-bit or more) pipelined DAC and an 8-bit+ pipelined ADC. The prototype design was fabricated in a standard low-cost 2 μm CMOS process.

For communication applications, high speed DACs are often required, especially in direct digital frequency synthesizers (DDFS) which are used in different modulation schemes for generating precise, spectral pure signals. In this dissertation a new method is proposed for designing low power and small area ROMless direct digital frequency synthesizers. In this method, a non-linear digital-to-analog converter is used to replace the phase-to-sine amplitude ROM look-up table and the linear DAC in conventional DDFS. Since the non-linear DAC converts the phase information directly into an analog sine wave, no phase-to-amplitude ROM look-up table is required [3] [4]. The conventional DDFS and its shortcomings, as well as the

proposed low-power DDFS architecture and its design procedure are presented in chapter 3. The detailed design of the nonlinear DAC is also presented in this chapter. To demonstrate this concept, two prototype DDFSs will be discussed.

Since data converters are used in many different applications and low power dissipation is usually required, new low voltage and low power techniques have to be investigated to satisfy these requirements. In chapter 4, a new low voltage technique based on biased inverting opamps that can have almost rail-to-rail swing with continuously valid output is discussed [5]. Based on the proposed biasing technique, a 10-bit segmented R-2R DAC and an 8-bit successive approximation ADC are designed and presented [6]. The basic concept of the biased inverting opamp technique as well as practical consideration in designing low voltage analog circuits will be discussed in this chapter.

In the last chapter, a summary of this research work, as well as the results and contributions are presented.

# CHAPTER 2. RECONFIGURABLE DATA CONVERTER

In this chapter the issues of integration and programmability in reducing power dissipation are addressed. The general goal of this chapter is to develop techniques at both the architecture and circuit design levels that enable both integration and programmability to minimize power dissipation in data converter applications.

Many digital systems require several data converters to communicate with the outside world because most input and output signals are analog in nature. Not all of these data converters are used at the same time. In this chapter, we present an architecture that can be programmed as an analog-to-digital converter (ADC), a digital-to-analog converter (DAC), or both. This reconfigurable data converter (RDC) can trade off between speed, power and resolution. RDC can save power by allowing the designer to program it as the right converter for a desired application. For example, such a converter can be used in combination with field programmable gate arrays (FPGAs) to implement field-programmable mixed analog and digital Arrays. These arrays can be used for prototyping mixed-signal circuits. Also the FPGA can be used for digital self-calibration of the RDC to improve its linearity. The RDC can convert an analog input signal to digital form. The digital signal can then be processed

by FPGA. The RDC can also convert the digital output of the FPGA back to analog form. As a result, the RDC gives the FPGA the power to communicate with the analog world. This application is explained in more detail in section 2.1. The flexibility of the RDC to be programmed as an ADC or a DAC enables us to use it for AC and DC tests similar to the case of using analog test buses and analog boundary scan. Furthermore, it allows digitized analog signals to be observed and controlled via test buses, similar to the mixed-mode boundary scan techniques. Therefore, it combines the advantages of both analog test buses and boundary scan techniques while the area overhead of the proposed techniques is very low compared to the mixed-mode boundary scan techniques. This application will be discussed in section 2.2. RDC can also be used as a stand-alone package to give flexibility to the user to choose ADC/DAC combinations for the desired application or in large mixed-mode systems where not all the converters are always in use.

## 2.1 RDC Applications in FPGA

FPGAs have already established their place in the digital design of prototype circuits and field-programmable analog arrays (FPAAs) have been recently introduced for prototyping analog circuits [7] [8] [9] [10]. To extend the application of FPAAs for prototyping mixed-signal circuits, one can create a field-programmable mixed analog and digital array by integrating an FPAA and an FPGA on a single chip [11] [12]. One of the most crucial components in such a concept is a data converter for

exchanging analog and digital signals between the FPAA and the FPGA [11] [13]. Since the requirements for speed, resolution, and accuracy vary for different mixed-signal systems, the data converter must be capable of reconfiguring under different conditions. The proposed RDC can satisfy these requirements.

Placing an RDC inside an FPGA chip gives the FPGA the power to communicate with the analog world. At the same time, the FPGA can be used to control and/or program the RDC. Such integration of RDCs with FPGAs also enables us to improve the accuracy of the RDC using a fully digital self-calibration technique, as we will discuss in section 2.4.

## 2.2 RDC for Mixed Signal Test

Boundary scan is the application of a scan path to the internal signal pins of an IC to provide controllability and observability to these pins. The process is well developed for testing digital circuits, but a structural test of analog and mixed-signal circuits is still under development. Recently, several design-for-test techniques (DFT) for mixed-signal systems have been proposed. These techniques utilize analog test buses [14] [15] [16], mixed-mode boundary scan [17] [18], and built-in self-test [19]. These techniques, except those that use analog test buses, usually require ADCs and DACs, which are assumed to be available in very large mixed-signal systems. However, many mixed-signal systems contain either ADCs or DACs but not both.

Incorporating additional data converters for DFT increases the area overhead and power dissipation.

Figure 2.1 shows a sample architecture using RDC for mixed-signal test applications. The RDC consists of a number of programmable data converter cells (PDCCs). The detailed design of the PDCCs is presented in the next section. Each PDCC can be programmed to operate as a divide by two ($x2^{-1}$), multiply by two (x2), or sample and hold (S/H). The PDCCs are connected in a cycle. Each PDCC is also connected to A/Din and A/Dout, the input and output analog/digital test buses. Using PDCCs, the digitized outputs of analog input peripheral circuits can be observed at the external pins via the boundary scan shift register and the digitized analog input to the analog output peripheral circuits can also be provided via boundary scan shift register. As a result, both controllability and observability for testing the analog circuits are provided. However, both ADCs and DACs are required to be connected to

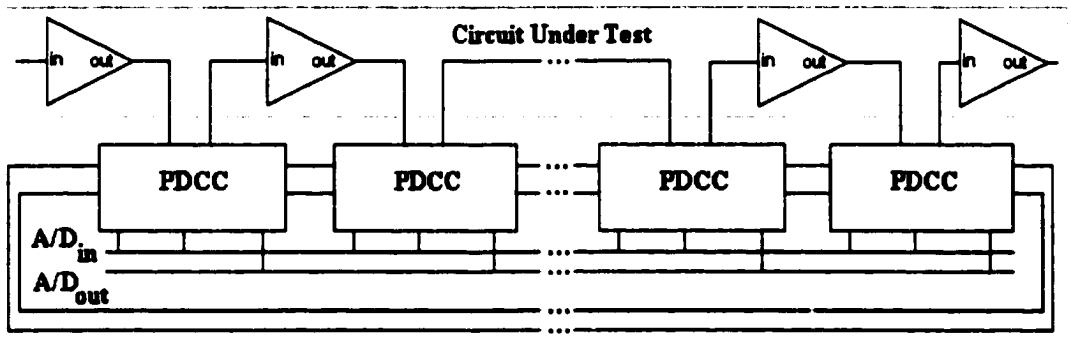



**Figure 2.1. Sample converter-test architecture for mixed-signal test**

the boundary scan shift register. Therefore, in mixed-signal systems that require only ADC or DAC for normal operation, additional data converters have to be added.

The reconfigurability of the RDC to different numbers of ADCs and DACs having different speeds and resolutions makes it an ideal choice for analog test bus, mixed-mode boundary scan, and built-in self test applications. The proposed RDC requires an area slightly larger than a conventional pipelined ADC with identical stages. Therefore, the area overhead for mixed-signal circuits that use ADCs and DACs is greatly reduced. For the same reason, the power dissipation is also reduced. However, it should be mentioned that in a conventional pipelined ADC the accuracy requirement is the highest for the first stage and the lowest for the last stage. Since a more accurate stage requires larger opamps and better-matched capacitors, it will occupy more area compared to the other stages. On the contrary, the RDC requires equal size cells with the accuracy requirement determined by the first stage. As a result, for large number of conversion bits the conventional pipelined ADC may be much smaller than the RDC.

## 2.3 Programmable Data Converter Cell (PDCC)

We first present a programmable data converter cell (PDCC) that can be used as a building block for data conversion applications in mixed-signal circuits. Then we will present the RDC using PDCCs and a programmable switching network to connect the cells together.

For simplicity, we use equations and schematics for single ended design, but in practice the whole design is fully differential to minimize some noise problems.

### 2.3.1 PDCC configured as a DAC cell

The analog output voltage of an N-bit DAC for the binary input $B_0\ B_1 \ldots B_{N-1}$ is given by:

$$V_{out} = \{ \sum_{0}^{N-1} Bj\ 2^{-j-1} \} V_{ref} \qquad (2.1)$$

where $V_{ref}$ is the reference voltage and $B_j$'s are assumed to be either equal to 0 or 1 in single ended designs, or equal to 1 or −1 in fully differential designs. The above equation can be rewritten as:

$$V_{out} = \{((\ldots(((B_{N-1}/2)+\ldots)+B_1)/2)+ B_0)/2\} V_{ref} \qquad (2.2)$$

This equation shows that the N-bit DAC can be built by cascading N identical DAC stages, which are realized by programming the cells. Each PDCC in DAC mode will consist of an adder and an amplifier stage with gain equal to $2^{-1}$. The output of each cell, $V_j$, can be described using the following equation:

$$V_j = ( V_{j-1} + B_j\ V_{ref} ) / 2 \qquad (2.3)$$

Figure 2.2 shows a switched-capacitor circuit that can perform $x2^{-1}$ required for a DAC operation. $\phi 1$ and $\phi 2$ are non-overlapping clock signals. The circuit samples the output voltage of the previous stage ($V_{j-1}$) during $\phi 1$ and produces the output voltage during $\phi 2$ according to equation 2.3. In a pipelined DAC, the outputs

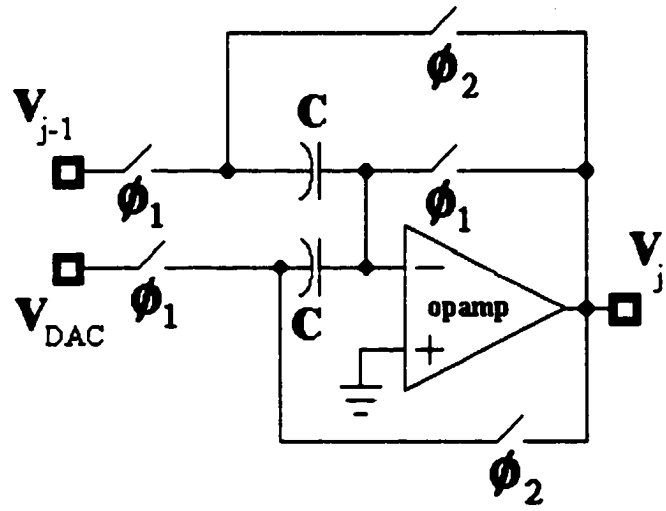



**Figure 2.2. PDCC configured as a DAC cell**

of each conversion stage in evaluating phase must be connected to the input of the next conversion stage that is in sampling phase. In other words, the clock signal $\phi 1$ in one stage is the clock signal $\phi 2$ in the next stage. Since the analog input to the first cell (the cell that receives the LSB from digital input) is zero, its input (both inputs for fully differential design) is switched to ground. The input bits ($B_j$'s) are sequentially applied to each $x2^{-1}$ cell starting form the LSB.

### 2.3.2 PDCC configured as an ADC cell

For an ideal N-bit ADC, the following equation relates the analog input signal $V_{in}$ to the digital output $B_{out} = B_1 B_2 \ldots B_N$:

$$V_{ref}(B_1 2^{-1} + B_2 2^{-2} + \cdots + B_N 2^{-N}) = V_{in} +/- V_{err} \qquad (2.4)$$

where $V_{ref}$ is the reference signal and $V_{err}$ is the conversion error voltage [20]. If we define $V_{LSB}$ to be the signal change corresponding to a single LSB change, then $V_{err}$ will be between -½ $V_{LSB}$ and ½ $V_{LSB}$ . For an N-bit ADC with a pipeline of N identical one-bit stages, the first stage compares the analog input signal to $V_{ref}/2$ to determine the MSB of the digital output. Each following stage doubles the error voltage of the previous stage and compares it to the $V_{ref}$ to determine the digital output bit of that stage. Therefore, the relationship between the output $V_j$ of the j-th stage and its input $V_{j-1}$ can be written as:

$$V_j = 2\,V_{j-1} - B_j\,V_{ref} \qquad (2.5)$$

Figure 2.3 shows a circuit that can perform the multiply by 2 (x2) operation needed for each ADC stage. Comparators determine the digital outputs and the switched-capacitor amplifier performs the multiply by 2 and the subtraction. Similar to the discussion for the DAC cell, the output of each conversion stage in a pipelined ADC in evaluating phase must be connected to the input of the next conversion stage which is in sampling phase. Therefore, the clock signal $\phi 1$ in each stage of the ADC is the clock signal $\phi 2$ in the next stage.

### 2.3.3 PDCC configured as a S/H cell

For S/H application, the output of each cell in the hold phase, $V_{out}$, should be equal to its input, $V_{in}$, in the sample phase. The switched-capacitor circuit in Figure

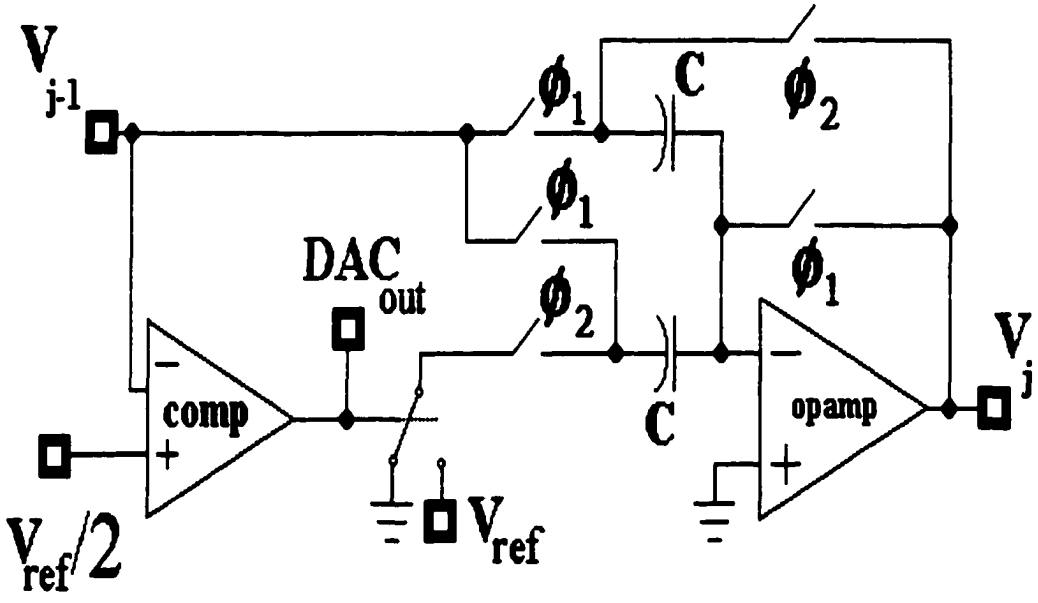



**Figure 2.3. PDCC configured as an ADC cell**

2.4 with a unity gain can perform the S/H operation.

### 2.3.4 The proposed PDCC

Figure 2.5 shows the proposed schematic of the PDCC (single ended). It consists of two capacitors, an opamp, a comparator, and ten switches which determine the modes of operation. The actual differential cell has one differential-in/differential-out opamp, one comparator, four capacitors, and nineteen switches (all capacitor and switches are doubled except for the switch at the output of the comparator). In comparison to the conventional pipelined ADC cell, the proposed PDCC design requires the same number of capacitors, opamps, comparators, and a few more logic gates. Hence, the PDCC requires an area that is approximately the same as an ADC

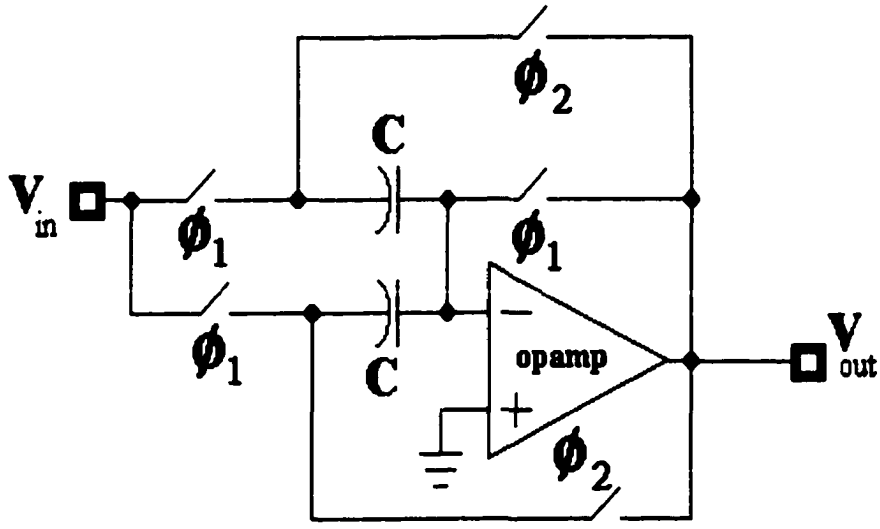



**Figure 2.4. PDCC configured as a S/H cell**

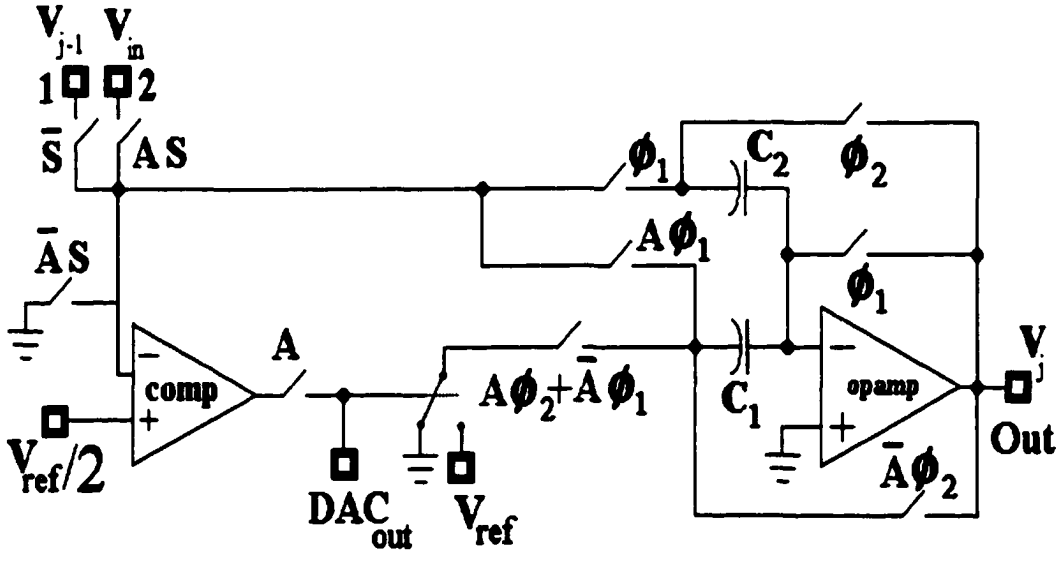



**Figure 2.5. The proposed programmable data converter cell**

cell being used as the first stage (MSB) of a pipelined ADC. The proposed PDCC can be programmed as any of the circuits in Figures 2.2-2.4 by choosing proper digital control signals for A and S. Table 2.1 shows the states of the switches for different modes of operation of a PDCC. The on and off states of the switches are labeled as 1 and 0, respectively. The analog input $V_{j-1}$ is the input from the previous PDCC and $V_{in}$ is the external analog input to the RDC. The $V_{in}$ input is only applied to the first PDCC (S=1) in ADC mode (A=1). The two non-overlapping clock signals $\phi 1$ and $\phi 2$ are provided by a clock distributor circuit and will switch places for adjacent cells. If we slightly reduce the gain of each stage of a pipelined ADC from 2, digital error correction can be used to improve the accuracy of the ADC. In our final RDC design, a control signal is used to add two small capacitors in parallel with the capacitors that are marked C2 in the single ended representation of Figure 2.5. Adding these capacitors will result in a gain of 1.93 and digital error correction can be applied.

**Table 2.1. Switch states for different operating modes of PDCC**

| operating mode | S | A |
|---|---|---|
| S/H | 1 | 1 |
| ADC | 0 | 1 |
| DAC lsb | 1 | 0 |
| DAC other bits | 0 | 0 |

The detailed design of the fully differential opamp and comparator that we used in the PDCC are shown in Figures 2.6 and 2.7. The opamp has a fully differential folded-cascode architecture with a common-mode feedback circuit. The fully differential comparator consists of two differential pair stages, a switched latch, a Schmitt trigger output stage, and the bias circuit. The bias circuits of the opamps and comparators are shared by all the PDCCs in the RDC.

### 2.3.5 Simulation results for PDCC

Three different modes of operations, namely, S/H, DAC, and ADC were simulated. In these simulations, the clock signal $\phi 1$ represents the sampling phase and

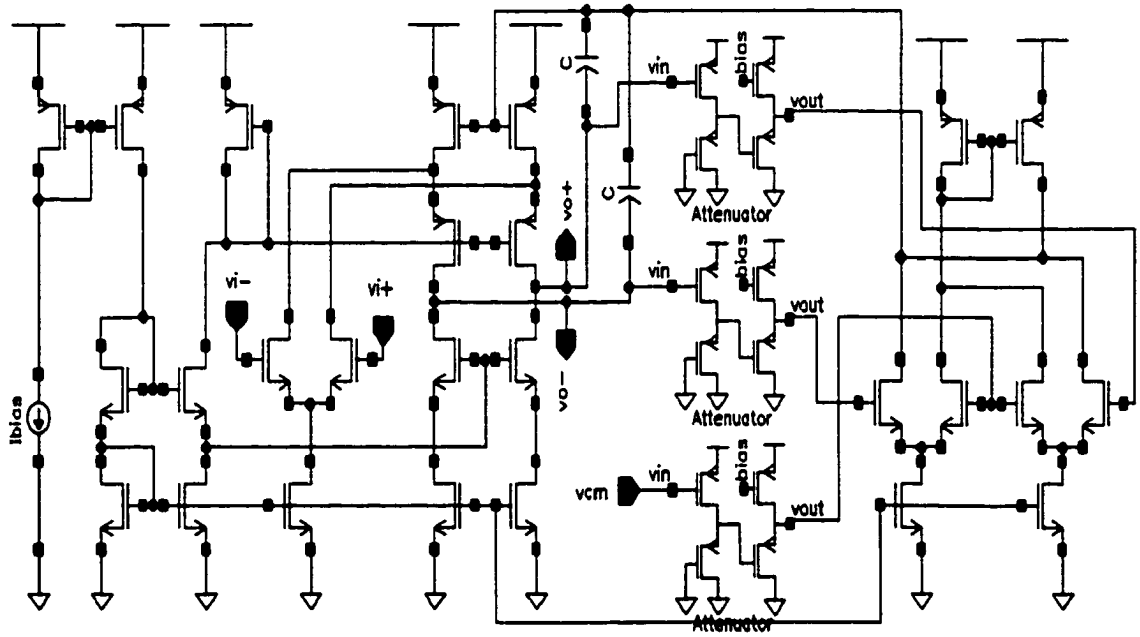



**Figure 2.6. Fully differential opamp used in the PDCC**

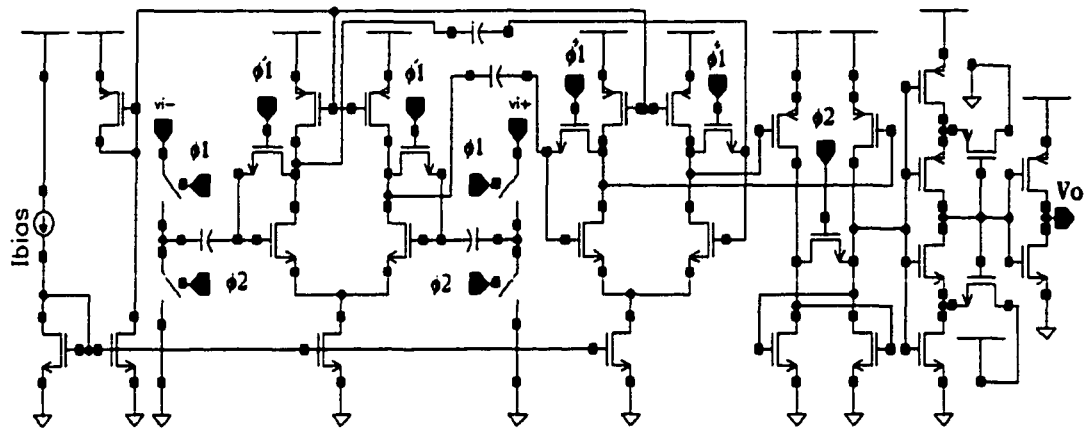



**Figure 2.7. Fully differential comparator used in the PDCC**

the clock signal $\phi 2$ represents the evaluating phase. To have proper operations, when the cells are connected as a pipelined DAC or ADC, the outputs of each conversion stage in evaluating phase must be connected to the input of the next conversion stage which is in sampling phase. In other words, the clock signal $\phi 1$ in one stage is the clock signal $\phi 2$ in the next stage.

Simulation results for the PDCC, designed in a fully differential architecture for three different modes of operation, i.e., S/H, ADC (multiply by two), and DAC (divide by two), are given in Figures 2.8-2.10. The single-ended input and outputs in addition to the differential output are shown. In Figure 2.8, we expect the differential output of the S/H amplifier to be settled to the differential input during $\phi 2$. The simulation result shows that a 0.6V differential input will result in a differential output of 598mV. The output settles within 0.1% of its final value in 33nsec. So the

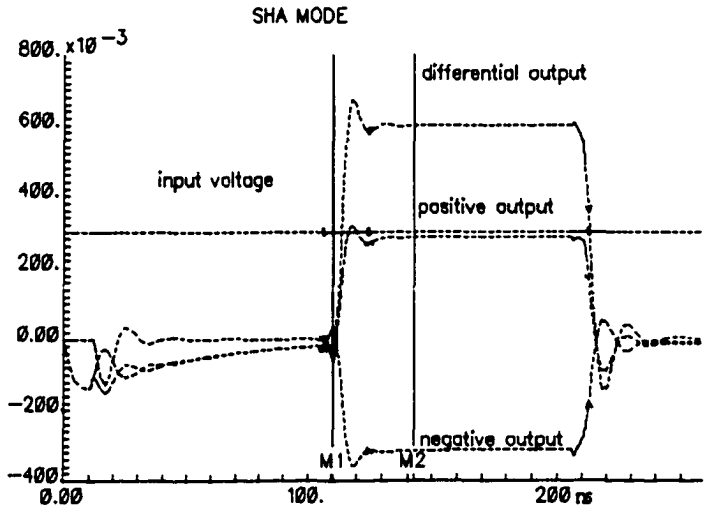



**Figure 2.8. Simulation result for S/H cell**

S/H is ideally able to provide 10-bits accuracy at a sampling frequency of 15 MHz (half period = 33nsec). Considering the non-ideal effects such as noise, mismatch, and parasitic capacitance, the actual accuracy and speed will be less. It will be discussed in more detail in section 2.6.

From equation 2.5, the input-output relationship for a pipeline of one-bit-per-stage fully differential ADCs is given by:

$$Vout_{diff} = 2Vin_{diff} - B\ Vref_{diff} \qquad (2.6)$$

where $Vout_{diff}$ is the differential output of the ADC cell, $Vin_{diff}$ is the differential input, and $Vref_{diff}$ is the differential reference voltage to be added or subtracted depending on the previous digital output bit. The output bit B in equation 2.6 is either -1 or 1 instead of 0 or 1 in the single ended case of equation 2.5. In Figure 2.9, the

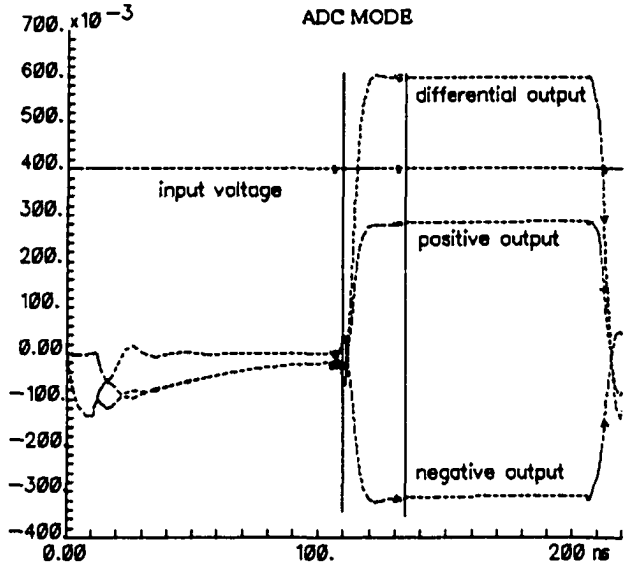



**Figure 2.9. Simulation result for ADC cell**

simulation results show that a 0.8V differential input will result in a differential output of 598mV, which is very close to the expected value of 0.6V for a 1V differential reference voltage. The output settles within 0.1% of its final value in 23nsec.

For a pipeline of one-bit-per-stage fully differential DACs, the input-output relationship for each stage is given by:

$$Vout_{diff} = (Vin_{diff} + B\ Vref_{diff})/2 \qquad (2.7)$$

As in equation 2.6, the digital bit B is either –1 or 1 for fully differential case. In Figure 2.10, the simulation results show that a 0.6V differential input will result in a differential output of 798.2mV for a 1V differential reference voltage and B=1. The simulation result is very close to the ideal output of 0.8V according to equation 2.7.

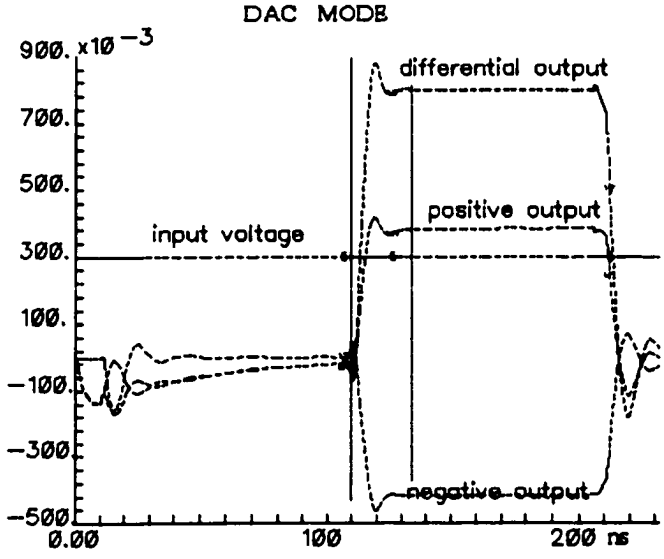



**Figure 2.10. Simulation result for DAC cell**

The output settles within 0.1% of its final value in 38.5nsec.

The simulated 0.1% settling time for different operating modes of the PDCC are summarized in Table 2.2. From the table we can see that the output of the ADC cell settles faster than the outputs of the S/H and DAC cells. This can be due to the fact that during $\phi 2$ the output of the ADC cell is connected to only one capacitor, while the outputs of the S/H and DAC cells are connected to two capacitors. Based on the simulation results, these cells can be used to realize data converters up to about 10-bit accuracy. Considering the loading effect of the switching network and the non-ideal effects such as noise, mismatch, and parasitic capacitance, the actual accuracy and speed will be less. As we will see in more detail in section 2.6, the tested data converters have about 8-bits of accuracy at close to 1MHz clock frequency.

**Table 2.2. Simulated 0.1% settling time for different PDCC operating modes**

| Operating mode | Settling time (nsec) |
|---|---|
| S/H | 33.0 |
| ADC | 23.0 |
| DAC | 38.5 |

## 2.4 Reconfigurable Data Converter (RDC)

In the previous section, we presented a programmable data converter cell that can be used as a building block for data conversion applications in mixed-signal circuits. Now we present a programmable switching network to connect the cells together. The structure of the proposed RDC is shown in Figure 2.11. It consists of an array of eight PDCCs and the programmable switching network. This interconnection network divides the PDCCs into different groups. It also allows the outputs of the PDCCs (labeled as out) to be fed as inputs to other cells (input 1). In a pipelined data converter, the output of each conversion stage in its evaluating phase must be connected to the input of the next conversion stage that is in its sampling phase. In other words, the clock signal $\phi 1$ in one stage is the clock signal $\phi 2$ in the next stage. In ADC mode, external analog inputs from analog I/O busses can be applied to the second input of each cell (input 2). In DAC mode, the analog output (out) of the cell corresponding to the last bit (MSB) will be connected to the analog I/O bus. For

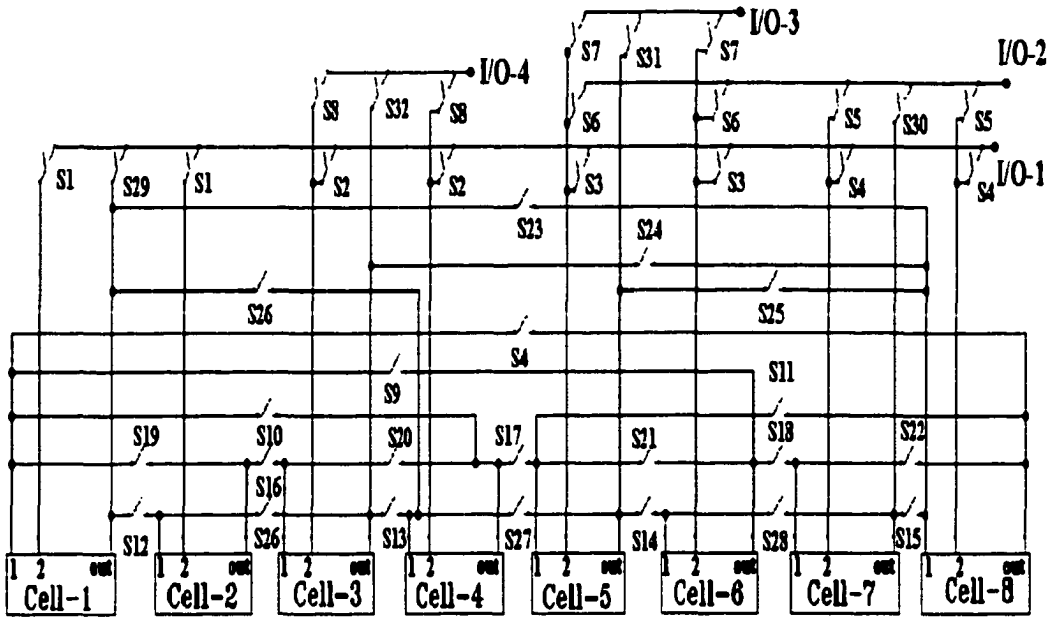



**Figure 2.11. Proposed RDC with eight PDCCs**

simplicity, digital input/outputs and control signals A and S to each cell are not shown in Figure 2.11. This structure can be programmed to perform different arbitrary bit DAC and/or ADC conversions. If N = number of conversion bits is larger than the number of available cells, the RDC can be programmed such that the output of the last cell can be applied back to the first cell to complete the conversion of N digital input bits. Therefore, the number of cells does not limit the resolution of the data converters but the accuracy of the ADC is dependent on the accuracy of each cell. Although the RDC requires N clock phases to complete the conversion of one sample in an N-bit conversion, the throughput is equal to 1 sample per ½ clock period. Since the clock phases between odd and even PDCCs are different, all the re-circulating ADCs or DACs must contain an even number of PDCCs.

Table 2.3 shows the switch states for different DAC and/or ADC conversions. In this table, A8 represents 8-bit or more (8-bit+) ADC, D8 represents 8-bit+ DAC, A62 represents a 6-bit+ ADC and a 2-bit+ ADC, etc. More PDCCs can be allocated to the converters that require high speeds and resolutions. High accuracy is achievable by applying self-calibration techniques without altering the architecture of the RDC. As proposed in [2], different DAC voltage outputs of a selected PDCC can be measured using the remaining PDCCs. The conversion results are then stored as digital coefficients in look-up tables during the calibration cycles. During the conversion cycles, these coefficients can be used to correct the errors of the PDCCs. As we mentioned before, this digital self-calibration technique can be implemented using an FPGA or a digital signal processor.

## 2.5 Reconfiguration Examples

In order to demonstrate the flexibility and reconfigurability of the proposed pipelined RDC architecture, we consider two different RDC configurations indicated by A8 (8-bit+ ADC) and D8 (8-bit+ DAC) on Table 2.3.

### 2.5.1 Prototype RDC configured as an 8-bit ADC

Figure 2.12 shows the RDC configured as an 8-bit+ ADC. For simplicity, only ON switches according to Table 2.3 are shown. In this case, during the 1$^{st}$ clock phase, the external analog input from I/O-1 is applied to the input 2 of the first PDCC

**Table 2.3. Switch states for different RDC configurations**

| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | S13 | S14 | S15 | S16 | S17 | S18 | S19 | S20 | S21 | S22 | S23 | S24 | S25 | S26 | S27 | S28 | S29 | S30 | S31 | S32 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A8** | 1 | 1 | 1 | 1 | | | | | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | | | | | | | | | | |
| **A62** | 1 | 1 | 1 | | 1 | | | | 1 | | | 1 | 1 | 1 | 1 | 1 | 1 | | | | | 1 | | | | | | | | | | |
| **A44** | 1 | 1 | | | 1 | 1 | | | | 1 | 1 | 1 | 1 | 1 | 1 | | | 1 | | | | | | | | | | | | | | |
| **A422** | 1 | 1 | | | 1 | | 1 | | | 1 | | 1 | 1 | 1 | 1 | 1 | | | | | 1 | 1 | | | | | | | | | | |
| **A2222** | 1 | | | | 1 | | 1 | 1 | | | | 1 | 1 | 1 | 1 | | | | 1 | 1 | 1 | 1 | | | | | | | | | | |
| **D8** | | | | | | | | | | | | | | | | | | | 1 | 1 | 1 | 1 | 1 | | | | 1 | 1 | 1 | 1 | 1 | 1 |
| **D26** | | | | | | | | | | | | 1 | | | | | | | 1 | 1 | 1 | 1 | | 1 | | | 1 | 1 | 1 | 1 | 1 | 1 |
| **D44** | | | | | | | | | | | | | | | | | | | 1 | 1 | 1 | 1 | | | 1 | 1 | | 1 | 1 | 1 | 1 | 1 |
| **D224** | | | | | | | | | | | | 1 | 1 | | | | | | 1 | 1 | 1 | 1 | | | 1 | | | 1 | 1 | 1 | 1 | 1 |
| **D2222** | | | | | | | | | | | | 1 | 1 | 1 | 1 | | | | 1 | 1 | 1 | 1 | | | | | | | 1 | 1 | 1 | 1 |
| **A6 D2** | 1 | 1 | 1 | | | | | | 1 | | | 1 | 1 | 1 | 1 | 1 | 1 | | | | | | | | | | | | | 1 | | |
| **A2 D6** | 1 | | | | | | | | | | | 1 | | | | | | | 1 | 1 | 1 | 1 | | 1 | | | 1 | 1 | | 1 | 1 | 1 |
| **A4 D4** | 1 | 1 | | | | | | | | 1 | | 1 | 1 | | | 1 | | | | | 1 | 1 | | | 1 | | | 1 | | 1 | 1 | |
| **A22 D4** | 1 | | | | | | | 1 | | | | 1 | 1 | | | | | | 1 | 1 | 1 | 1 | | | 1 | | | 1 | | 1 | 1 | |
| **A4 D22** | 1 | 1 | | | | | | | | 1 | | 1 | 1 | 1 | 1 | 1 | | | | | 1 | 1 | | | | | | | | 1 | 1 | |
| **A222 D2** | 1 | | | | | | 1 | 1 | | | | 1 | 1 | 1 | 1 | | | | 1 | 1 | 1 | 1 | | | | | | | | 1 | | |
| **A2 D222** | 1 | | | | | | | | | | | 1 | 1 | 1 | 1 | | | | 1 | 1 | 1 | 1 | | | | | | | | 1 | 1 | 1 |
| **A42 D2** | 1 | 1 | | | | | 1 | | | 1 | | 1 | 1 | 1 | 1 | 1 | | | | | 1 | 1 | | | | | | | | 1 | | |
| **A2 D24** | 1 | | | | | | | | | | | 1 | 1 | | | | | | 1 | 1 | 1 | 1 | | | 1 | | | 1 | | 1 | 1 | 1 |
| **A22 D22** | 1 | | | | | | | 1 | | | | 1 | 1 | 1 | 1 | | | | 1 | 1 | 1 | 1 | | | | | | | | 1 | 1 | |

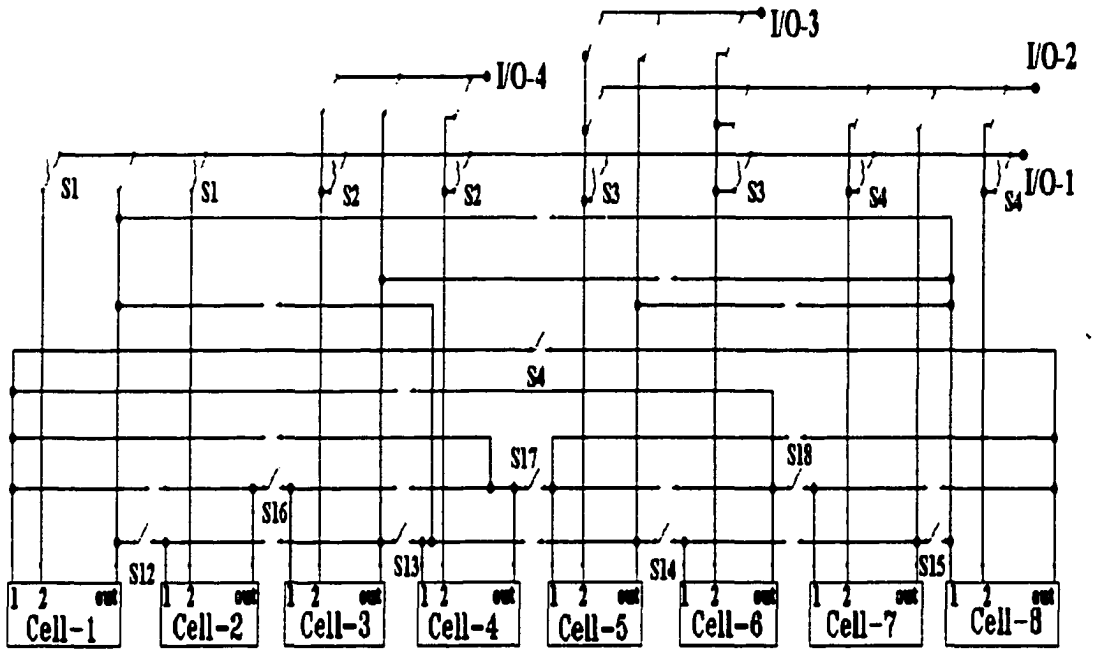



**Figure 2.12. Prototype RDC configured as an 8-bit+ ADC**

(cell-1). During the 2nd clock phase, the analog output of cell-1 is calculated according to equation 2.5 and is applied to the input 1 of cell-2 and so on. The output of the last cell (cell-8) is fed back to the input 2 of the first cell to enable the circuit to perform as an ADC with more than 8 conversion bits.

### 2.5.2 Prototype RDC configured as an 8-bit DAC

Figure 2.13 shows the RDC configured as an 8-bit+ DAC. The input bits ($B_j$'s) are sequentially applied to each $x2^{-1}$ cell starting form the least significant bit (LSB) $B_{N-1}$. First, the LSB of the digital input is applied to cell-2. Since the analog input to

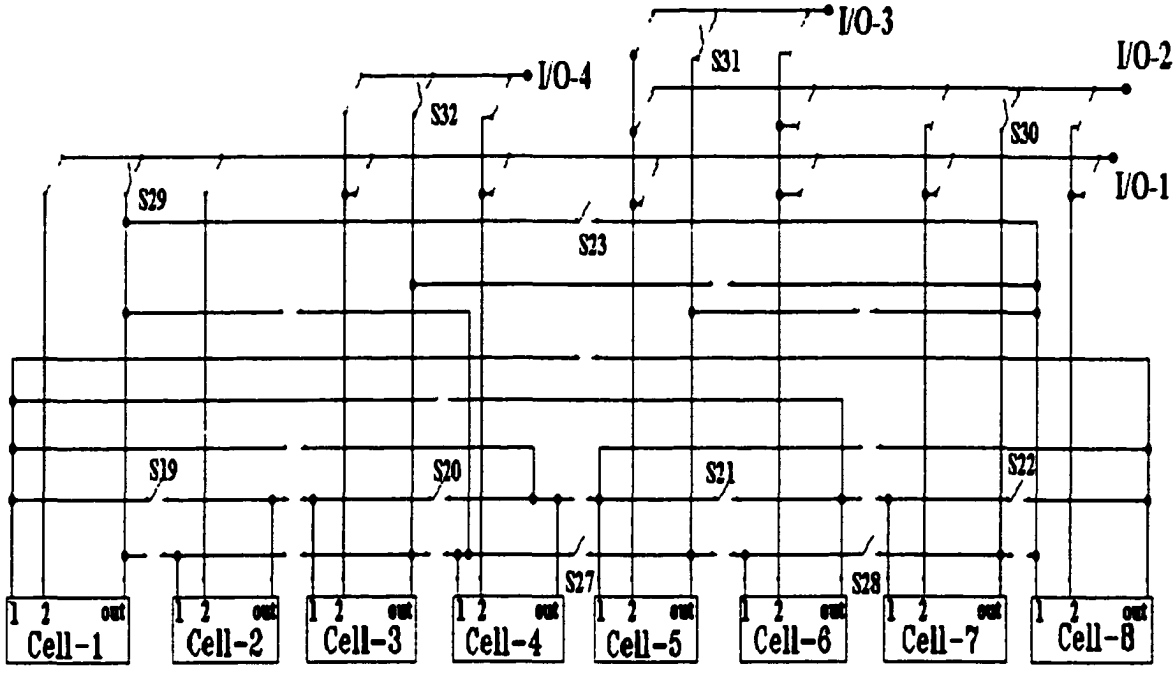



**Figure 2.13. Prototype RDC configured as an 8-bit+ DAC**

this cell is zero, its input is switched to ground (both inputs for fully differential design). During the 2nd clock phase, the analog output of cell-2 is calculated according to equation 2.3 and applied to the input 1 of cell-1. At the same time, the 2nd LSB of the digital input is applied to the digital input of cell-1. During the 3rd clock phase the analog output of the cell-1 and the 2nd LSB of the digital input are applied to cell-8 and so on. Finally, during the eighth clock phase, the analog output of cell-4 and the MSB of digital input are applied to cell-3. The analog output of cell-3 is the conversion result of the 8-bit DAC. It will be applied to the analog I/O bus through I/O-4.

## 2.6 Test Results

The prototype RDC with eight PDCCs was designed and fabricated in a typical 2 μm CMOS process. Figure 2.14 shows the die photo of the prototype RDC. The active area of the chip is 2 mm by 4.9 mm. A Xilinx FPGA was used to program the RDC for different configurations. The RDC was configured as an 8-bit ADC and an 8-bit DAC as explained in section 2.5.

### 2.6.1 Test results of RDC configured as an 8-bit DAC

The RDC was first configured as an 8-bit DAC. DC measurement of the DAC was performed using HPVEE software, an 8-bit counter, HP8904A function generator, and HP34401 digital voltmeter. HPVEE controlled the function generator to provide a 1 Hz clock signal for the counter and the counter's 8-bit digital ramp output was applied to the input of the DAC. The DAC's analog output voltage, as read by a digital voltmeter, was saved in a file and used to measure the differential nonlinearity (DNL) and integral nonlinearity (INL) of the DAC. The DC test results of the DAC are shown in Figure 2.15.

For AC test of the DAC, a 1 kHz input signal was applied to a 12-bit commercial ADC (Linear Technology LTC1278) which has an INL = DNL = 1 LSB. The 8 MSB outputs of the ADC were applied to our 8-bit DAC. Figure 2.16 shows the output spectrum of the DAC for a 1 MHz clock (twice the recommended sampling frequency of LTC1278), as measured by a Tektronix 2710 spectrum analyzer. The

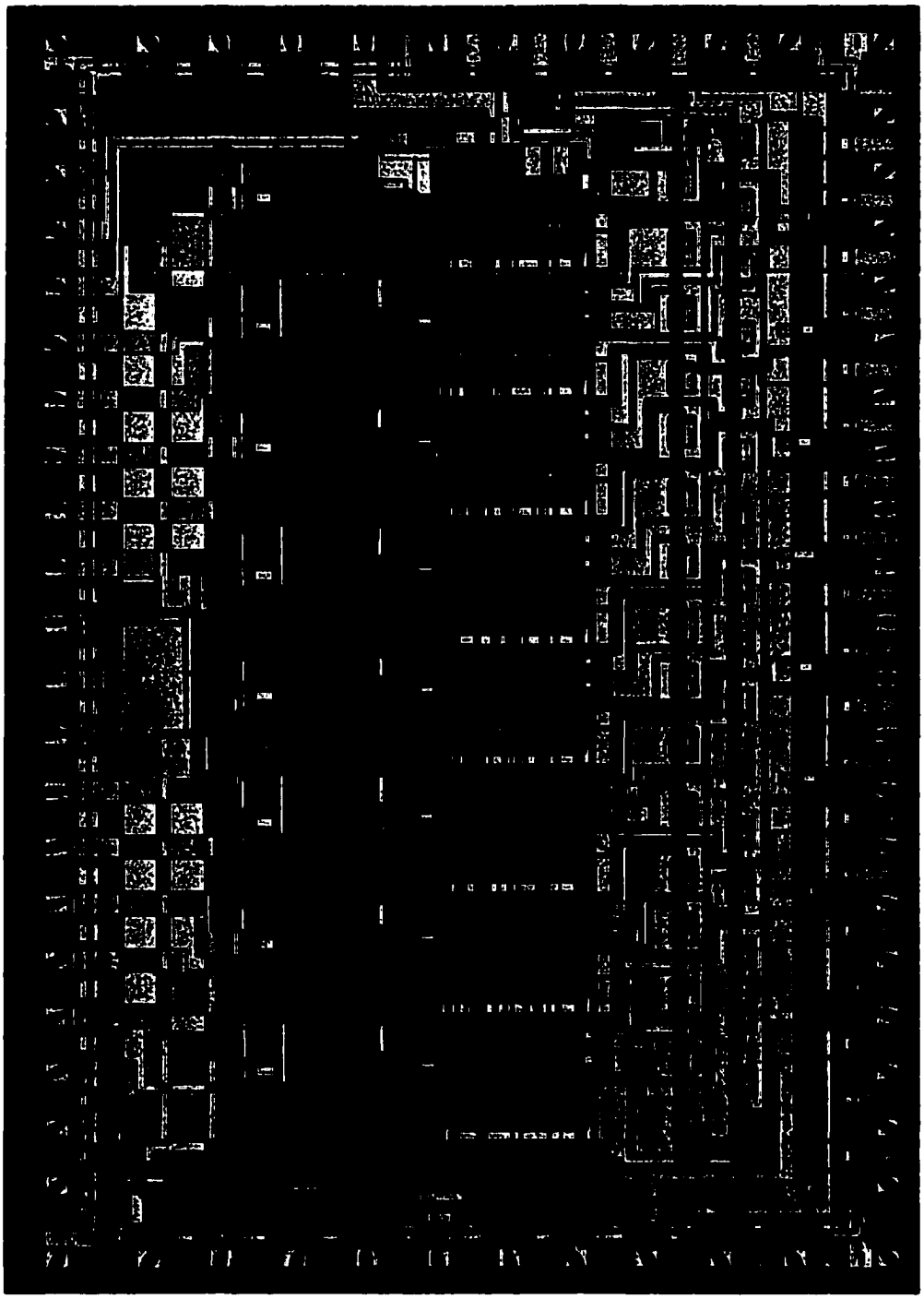


**Figure 2.14. Die photo for the prototype RDC**

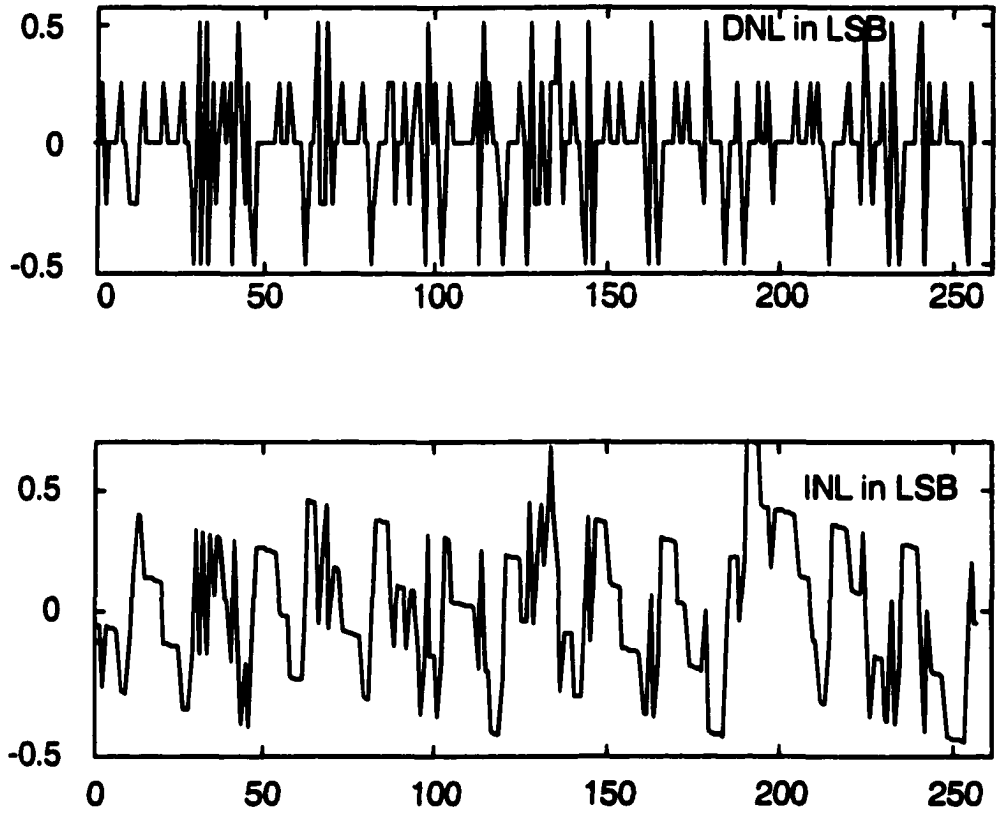



**Figure 2.15. DNL and INL for RDC configured as an 8-bit DAC**

output spectrum was used to calculate the spurious free dynamic range (SFDR), signal-to-noise plus distortion ratio (SNDR), and effective number of bits (ENOB). In these measurements, we assumed that the commercial ADC is ideal and all the nonlinearity and noise is due to our DAC. The measured ENOB of our DAC is 7.8 bits at 1 MHz clock rate. The difference between the measured results and the simulation results of section 2.3.5 is due to the voltage drop in the switching network and other non-ideal effects such as noise, mismatch, and parasitic capacitance. The test results for the 8-bit DAC are summarized in table 2.4.

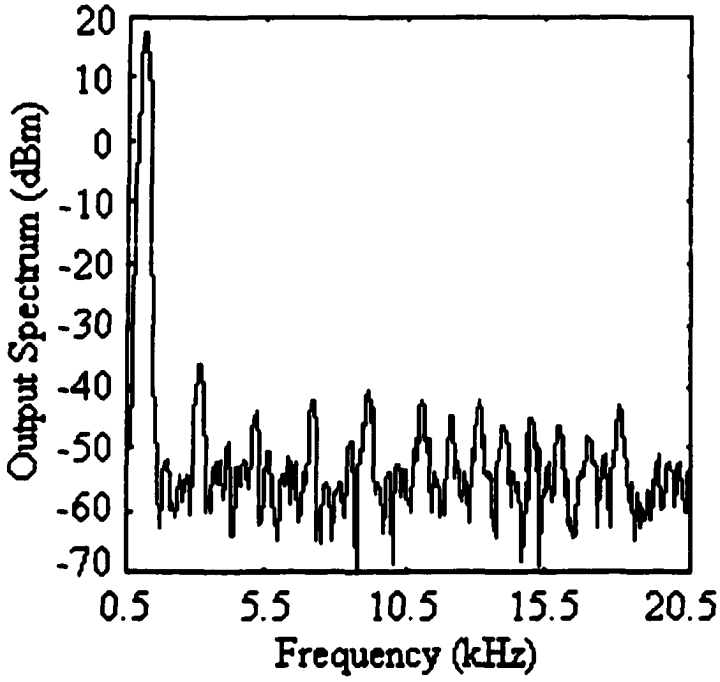



**Figure 2.16. AC test result of RDC configured as an 8-bit DAC for a 1 kHz input signal and 1 MHz clock**

**Table 2.4. Measured performance of the RDC configured as an 8-bit DAC**

| | |
|---|---|
| INLmax | 0.76 LSB |
| DNLmax | 0.50 LSB |
| SFDR@1kHz | 53.7 dB |
| SNDR@1kHz | 48.7 dB |
| ENOB@1kHz | 7.8 bits |
| Clock rate | 1 MHz |
| Supply voltage | 5 V |

### 2.6.2 Test results of RDC configured as an 8-bit ADC

The RDC was also configured as an 8-bit ADC. Code density measurement was used to measure the DNL and INL of the ADC. First, a very low frequency (0.1 Hz) ramp signal with a peak-to-peak amplitude of slightly more than the maximum input range of the ADC was applied to the input of the ADC. Then the digital output of the ADC was recorded using a Tektronix TLA711 logic analyzer. The digital code was used to measure the DNL and INL of the ADC. The DC test results for the ADC are shown in Figure 2.17.

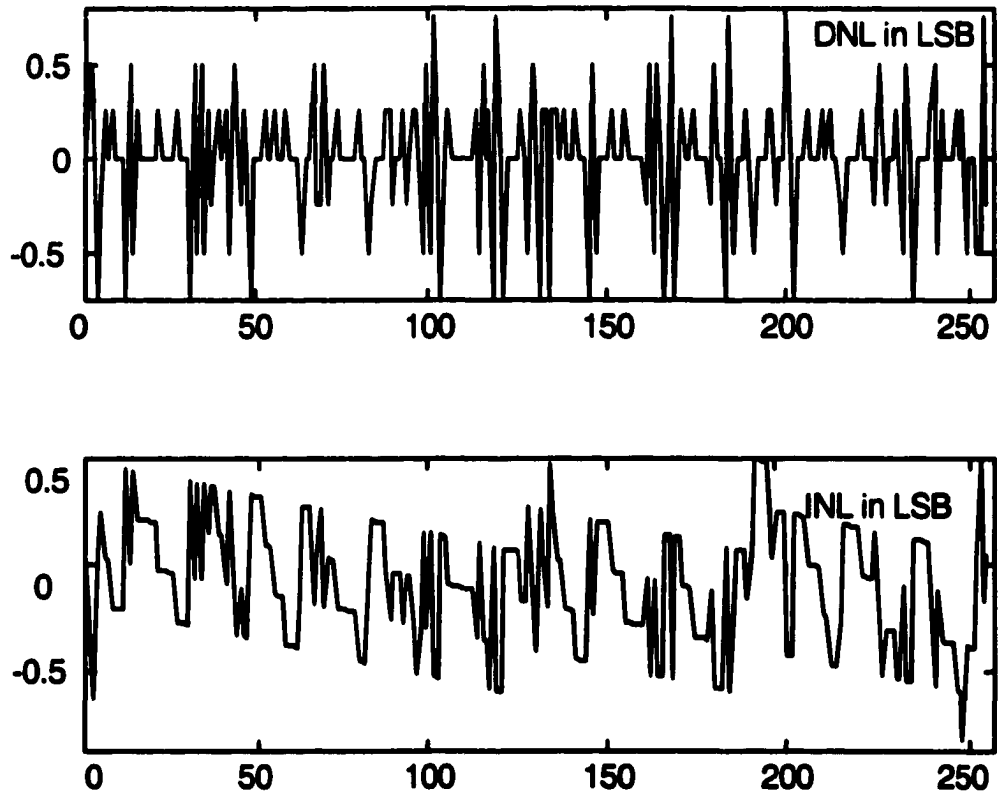



**Figure 2.17. DNL and INL for RDC configured as an 8-bit ADC**

For AC test of the ADC, a 1 kHz input signal was applied to the input of our ADC at a sampling rate of 1.25 MHz. The 8 output bits of our ADC were then applied to the 8 MSBs of a 12-bit commercial DAC (Maxim MAX507). The INL and DNL of MAX507 are 1 LSB and it settles within ½ LSB in 5 μsec. Figure 2.18 shows the output of the MAX507 as measured by a Tektronix 2710 spectrum analyzer. The output spectrum was used to calculate the SFDR, SNDR, and ENOB of our ADC. In these measurements, we assumed that MAX507 is an ideal DAC and all the nonlinearity and noise is due to our ADC. The measured ENOB of our ADC is 7.7 bits at 1.25 MHz clock rate. As we discussed before, the difference between the

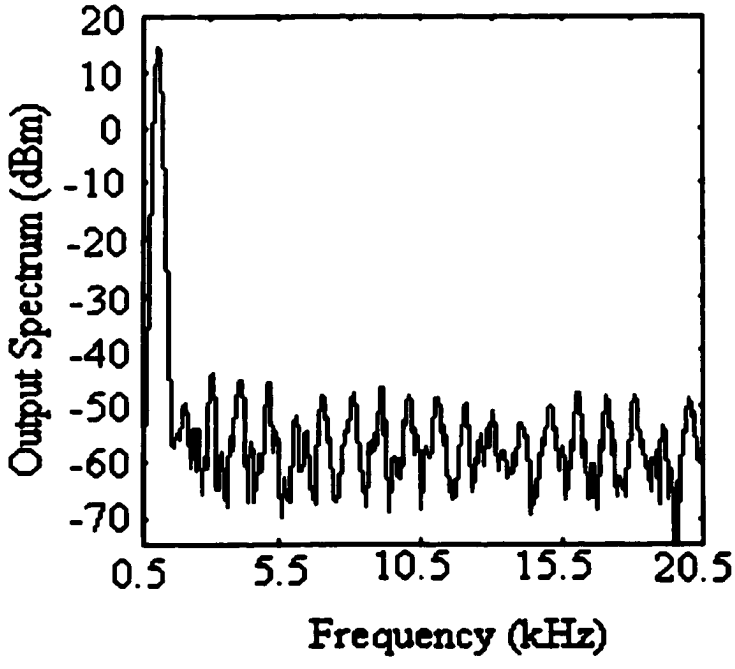



**Figure 2.18. AC test result of RDC configured as an 8-bit ADC for a 1 kHz input signal and 1.25 MHz clock**

measured results and the simulation results of section 2.3.5 is due to the loading effect of the switching network and other non-ideal effects such as noise, mismatch, and parasitic capacitance. The test results of the 8-bit ADC are summarized in table 2.5.

## 2.7 Summary

In this chapter, we presented a programmable data converter cell (PDCC) that can be programmed to operate as a divide by two ($x2^{-1}$), multiply by two (x2), or sample and hold (S/H). The cell was used as a building block in a reconfigurable data converter (RDC). This architecture is much more flexible than fixed data converters. We discussed some potential applications for the RDC in mixed-mode circuits such as analog boundary-scan and analog test bus. To show the programmability of the

**Table 2.5. Measured performance of the RDC configured as an 8-bit ADC**

| | |
|---|---|
| INLmax | 0.97 LSB |
| DNLmax | 0.74 LSB |
| SFDR@1kHz | 58.4 dB |
| SNDR@1kHz | 48.2 dB |
| ENOB@1kHz | 7.7 bits |
| Clock rate | 1.25 MHz |
| Supply voltage | 5 V |

RDC, a prototype RDC with 8 PDCCs was fabricated and tested. The test results for the RDC programmed as an 8-bit DAC and an 8-bit ADC are presented. As in other pipelined data converters, fully digital error correction (self-calibration) can be applied to RDC to improve its accuracy.

# CHAPTER 3. NON-LINEAR DAC FOR LOW-POWER DIRECT DIGITAL FREQUENCY SYNTHESIZERS

In this chapter, a design technique that uses nonlinear digital-to-analog converter (DAC) for implementing low-power direct digital frequency synthesizer (DDFS) is proposed. The nonlinear DAC is used in place of the ROM lookup table for phase-to-sine amplitude conversion and the linear DAC in a conventional DDFS. Since the proposed design technique for DDFS does not require a ROM, a significant saving in power dissipation has resulted. The design procedure for implementing the nonlinear DAC is presented. To demonstrate the proposed technique, two quadrature DDFSs, one using nonlinear resistor string DACs and the other using nonlinear current-mode DACs, were implemented. For a 3.3 V supply, the resulted power dissipation for both DDFSs are 4 mW and 92 mW at a clock rate of 25 MHz and 230 MHz, respectively. For both DDFSs, the spurious free dynamic ranges are over 55 dBc for low synthesized frequencies.

## 3.1 Introduction

Direct digital frequency synthesizers (DDFSs) play an important role in many communication systems. Traditionally, phase-locked loops (PLLs) are usually

employed in designing frequency synthesizers. High synthesized frequencies can be achieved using this approach. However, fast frequency switching is becoming critically important in modern wireless communication systems such as in spread-spectrum communication systems [21] [22]. Conventional PLL frequency synthesizers are usually not suitable for these applications due to the inherent feedback loop inside a PLL that prolongs the settling time during frequency switching. To achieve fast frequency switching, direct digital frequency synthesizers have been considered as an alternative to PLL frequency synthesizers since they do not have a feedback loop and hence, can provide fast frequency switching.

Other advantages of DDFS over a PLL approach include: low phase noise (roughly equal to that of the input clock), high frequency resolution, fast channel switching, continuous-phase switching, and allowing direct frequency and phase modulation in the digital domain [21] [22] [23] [24]. These properties are important in some modulation schemes. While DDFS provides the above features, it is considered to be power-hungry, especially for high clock frequency. Thus, it has not been widely used in portable wireless communication systems. Most of the power dissipation in a DDFS is mainly consumed in the conversion of phase information into sine amplitude that usually utilizes a large ROM lookup table and additional logic circuits.

In this chapter, a low-power technique using a nonlinear digital-to-analog converter (nonlinear DAC) is used to implement DDFS. Based on this technique,

significant power savings compared to conventional DDFS (more than a few times less power consumption) can be achieved. This will be demonstrated based on two prototype DDFSs as described in this chapter.

## 3.2 Conventional DDFS Architecture

The architecture of a conventional DDFS is originally introduced by Tierney et al [22]. It consists of the following basic building blocks – a phase accumulator, a phase-to-sine amplitude ROM look-up table, and a linear DAC as shown in Figure 3.1. During each clock cycle, the digital input phase increment $\Delta\phi$ is added to the data previously held in the phase accumulator $\phi(n)$. The phase accumulator operates on the principle of overflow arithmetic. For a given clock frequency $f_{clk}$, the rate of overflow, and hence the output frequency $f_{out}$, is given by $\Delta\phi \cdot f_{clk}/2^j$ where j is the number of bits of the accumulator and $\Delta\phi$ must be less than or equal to $2^{j-1}$. The phase accumulator addresses the ROM lookup table, which converts the phase information into the values of sine wave. The linear DAC is used to convert the quantized sine wave into analog voltage. In most DDFS implementations, the most significant bit (MSB) and the second MSB of the phase accumulator output are used to decode the quadrant of the sine function so that the ROM lookup table only needs to store sine information from 0 to $\pi/2$ radians. Furthermore, a ½ LSB offset is usually introduced to both the phase and the amplitude of the sine wave samples [25] such that the complementors can be realized as simple 1's complementors (XOR gates).

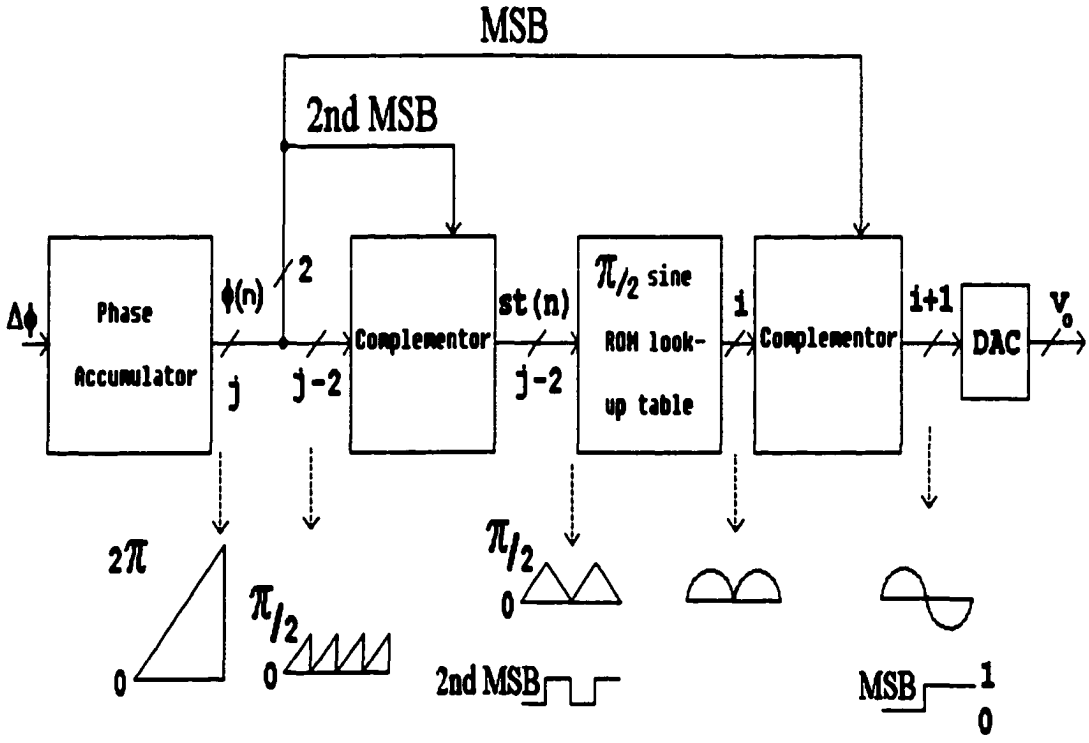



**Figure 3.1. Conventional ROM based DDFS**

Large ROM and high resolution DAC are usually required to improve the spectral purity of a sine wave output. However, a larger ROM lookup table means higher power consumption, lower reliability, slower access time and larger die area. Recently, efforts have been made to reduce the ROM size using different compression techniques, which include the use of trigonometric identity [26], the Nicholas technique [25], the use of Taylor series [27], and the CORDIC algorithm [28]. These techniques can be used to reduce the size of the ROM significantly (32 times or more [29]). However, digital adders and other extra digital circuits are often required. As a result, reducing the ROM size using these techniques may not result in significant

reduction in overall power dissipation. Furthermore, if quadrature DDFS is required, two ROM lookup tables and two linear DACs as shown in Figure 3.2 will be needed, and even higher power dissipation will be expected.

## 3.3 Proposed DDFS Architecture

A new architecture to implement DDFS is proposed as shown in Figure 3.3. In this architecture, a nonlinear DAC is used in place of the ROM lookup table and the linear DAC in a conventional DDFS [30] [3]. The function of the nonlinear DAC is to convert the digital phase information from the phase accumulator directly into an analog sine output voltage. The performance of the proposed architecture is theoretically identical to the performance of a conventional ROM based DDFS with the same number of phase resolution bits and the same number of amplitude resolution bits. The main advantage of the proposed architecture is that it does not

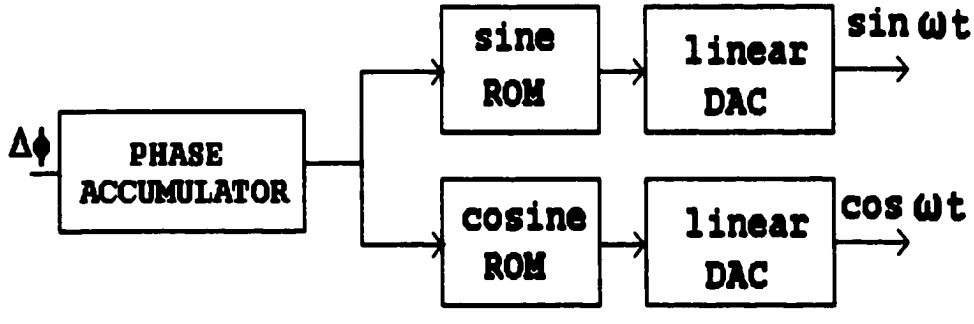



**Figure 3.2. Conventional quadrature DDFS architecture**

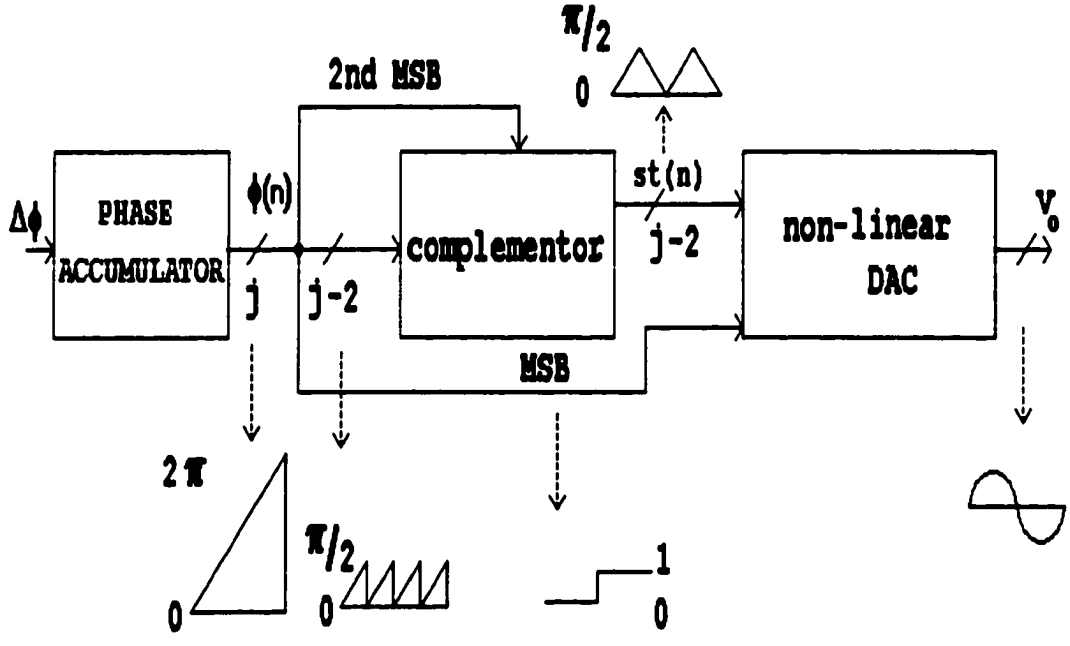



**Figure 3.3. Proposed DDFS architecture that uses nonlinear DAC**

require a ROM lookup table. Therefore, the power dissipation will be less than that of a conventional DDFS if the nonlinear DAC consumes about the same power as a linear DAC. To implement such a nonlinear DAC, one can use a linear DAC followed by a translinear sine converter [31], which utilizes the exponential characteristic of bipolar transistors. However, this approach can only be implemented in a BiCMOS or Bipolar technology and is not suitable for implementation in a conventional CMOS process. It will be more desirable to have a design technique, which is independent of the fabrication process. In the following section, such a design technique and the corresponding design procedure are described.

## 3.4 Nonlinear DAC Design

A method for designing the nonlinear DAC is proposed in this section. Referring to Figure 3.3, the output of the nonlinear DAC $v_o$ is a function of the complementor output st(n) and the MSB of the phase accumulator output $\phi(n)$. Assume that the peak value of the output sine wave is equal to $2^i$-1 where i defines the number of bits of amplitude resolution of the sine wave. Then, ideally, $v_o$ is given as

$$v_{o,ideal} = \begin{cases} (2^i - 1)\sin\left(\frac{st(n)}{2^{j-1}}\right) & \text{for} \quad MSB = 0 \\ -(2^i - 1)\sin\left(\frac{st(n)}{2^{j-1}}\right) & \text{for} \quad MSB = 1 \end{cases} \tag{3.1}$$

where $0 \le st(n) \le 2^{j-2}-1$. The integer j represents the number of MSB bits outputted from the phase accumulator that is used as input bits to the nonlinear DAC. The value of j can be less than or equal to the total number of bits provided from the phase accumulator. To have a practical nonlinear DAC realization, the nonlinear DAC is assumed to have $2^{j-2}$ DAC cells. For the k-th DAC cell where k = 0, ··· , $2^{j-2}$-1, the output is assumed to be an integer with a value of $o_k$. For a given value of st(n), the output of the nonlinear DAC $v_o$ is defined to be the summation of the DAC cell outputs from cells 0 to st(n) and can be written as

$$|v_o| = \sum_{k=0}^{st(n)} o_k \tag{3.2}$$

where the polarity of $v_o$ depends on the MSB of $\phi(n)$. Based on equations 3.1 and 3.2, the output value of the k-th DAC cell can be determined using the following iterative

equation where [·] denotes the operation of rounding a real number to its nearest integer.

$$o_k = \begin{cases} \left[ (2^i - 1)\sin\left(\frac{0.5}{2^{j-1}}\right) \right] & \text{for } k = 0 \\ \left[ (2^i - 1)\sin\left(\frac{k+0.5}{2^{j-1}}\right) - \sum_{m=0}^{k-1} o_m \right] & \text{for } 1 \le k \le 2^{j-2} - 1 \end{cases} \tag{3.3}$$

The value of 0.5 in the above equation is to introduce a ½ LSB offset to the phase and amplitude such that XOR gates can be used as 1's complementors as descried in Section 3.5. The above procedure for finding $o_k$ will produce errors on the output sine wave due to round off effects. However, integer values of $o_k$'s are desired so that good matching between DAC cells can be accomplished. In addition, the design and the layout of DAC cells can be simplified. For ideal nonlinear DAC cell outputs, the output sine wave will have equivalent accuracy when compared to the conventional DDFS with an ideal i-bit linear DAC and j input bits of phase resolution to the ROM lookup table.

From equation 3.3, it can be found that the minimum value of $o_k$ is usually equal to zero. However, the maximum value of $o_k$, $o_{max}$, is dependent on the values of j and i as shown in Table 3.1. The value of $o_{max}$ can always be obtained at or near k = 0 where the slope of the sine wave is at its maximum value equal to $(2^i\text{-}1)\pi/2^{j-1}$. As a result, the value of $o_{max}$ is equal to $\lceil (2^i\text{-}1)\pi/2^{j-1} \rceil$. It can be observed that $o_{max}$ almost doubles when i is increased by 1 bit and $o_{max}$ is reduced approximately by a

**Table 3.1. The value of $o_{max}$ for different values of i and j**

| | j = 10 | j = 11 | j = 12 | j = 13 |
|---|---|---|---|---|
| i = 8 | 2 | 1 | 1 | 1 |
| i = 9 | 4 | 2 | 1 | 1 |
| i = 10 | 7 | 4 | 2 | 1 |
| i = 11 | 13 | 7 | 4 | 2 |
| i = 12 | 26 | 13 | 7 | 4 |

half when j is increased by 1 bit. The value of $o_{max}$ will directly affect the size of the DAC cells since the size of each DAC cell will be unified to have the same size and to be proportional to $o_{max}$ number of unit resistors, or current sources, to simplify the layout of the entire nonlinear DAC. Further observation shows that, for a fixed amplitude resolution (i.e. for fixed i), the number of DAC cells doubles when j is increased by 1 bit. However, the area of each DAC cell will decrease by about a half[1] since $o_{max}$ decreases by almost a half. As a result, the overall area of the DDFS will

[1] The area of the DAC cell will reduce by almost a half if the area of the required digital circuit inside the cell is small.

only increase slightly for increasing the phase information to the nonlinear DAC (i.e. increasing the value of j). For conventional ROM based DDFS architecture, this is usually not the case since increasing the value of j by 1 bit means increasing the number of input address bits of the ROM by 1 bit and hence, doubling the ROM size. Therefore, the proposed architecture will have significant advantages in terms of power dissipation and die area over the conventional architecture for large phase resolution, which is required in many applications.

## 3.5 Prototype Quadrature DDFS Using Nonlinear Resistor String DACs

Based on the proposed technique, a quadrature DDFS was designed with the nonlinear DACs implemented using resistor string. Conceptually, the nonlinear DACs can be realized as shown in Figure 3.4a. The input signal st(n) and the MSB of the phase accumulator are first decoded so that only one of the switches will turn on and, hence, there is only one low impedance path between the resistor string and the input of the buffer. The resistance value in each DAC cell is equal to $o_k \cdot R$, and the total resistance of the entire resistor string is equal to $2^{i+1} \cdot R$ where R represents the unit resistance value. The output voltage of the nonlinear DAC can be written as:

$$v_o = \begin{cases} \dfrac{V_{ref}}{2^i R} \sum_{k=0}^{st(n)} o_k R & \text{for} \quad MSB = 0 \\ -\dfrac{V_{ref}}{2^i R} \sum_{k=0}^{st(n)} o_k R & \text{for} \quad MSB = 1 \end{cases} \tag{3.4}$$

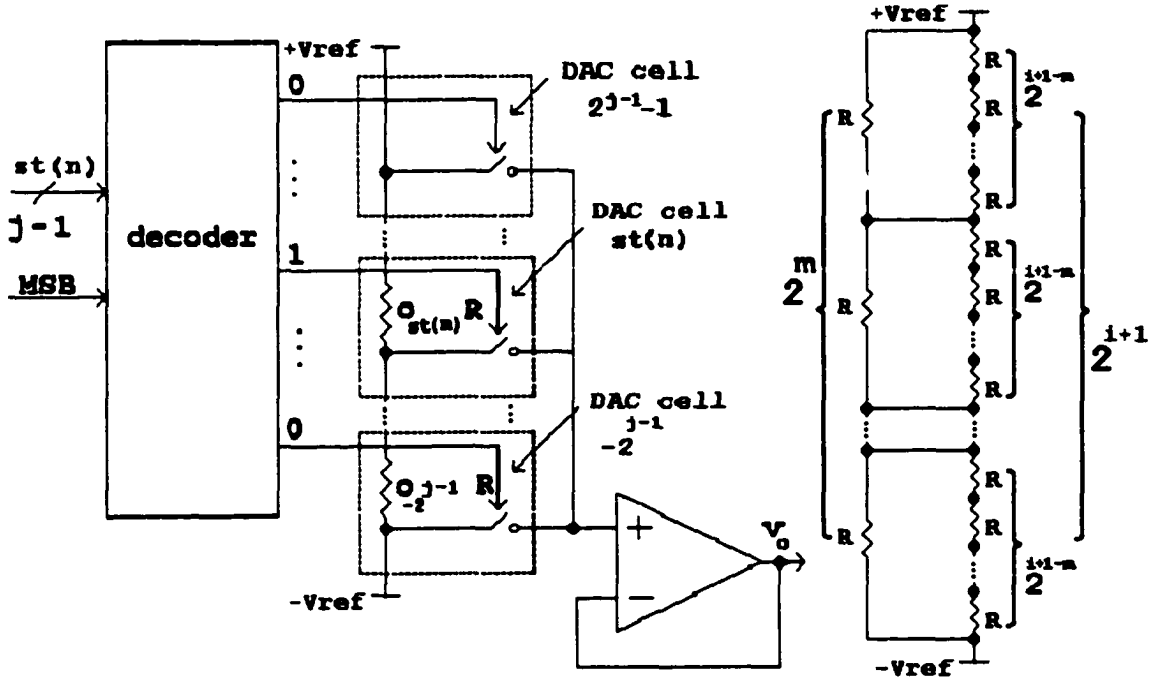



**Figure 3.4. (a) Nonlinear resistor string DAC and (b) low-ohmic resistor ladder**

Although each DAC cell layout size can be proportional to $o_k \cdot R$, it is unified to have the same size as $o_{max} \cdot R$ to simplify the layout of the entire nonlinear DAC.

If high amplitude resolution is required, the nonlinear DAC will require a long resistor string. As a result, the signal propagation delay for the nodes that are near the two reference voltages will be much less than the delay for the nodes at the middle of the resistor string, since nodes at different locations along the resistor string have different RC time constants. This effect may cause harmonic distortion at the output. To reduce this effect, a low-ohmic resistor ladder can be connected to the resistor string. The low-ohmic resistor ladder was chosen to have $2^m$ equal resistors of size R,

which is the same as the unit resistance of the original resistor string. As shown in Figure 3.4b, each resistor in the low-ohmic resistor ladder is in parallel with $2^{i+1-m}$ resistors in the original resistor string. Therefore, the maximum resistance of the resistor string, which corresponds to the node at the middle of the resistor string, will drop from $2^{i-1} \cdot R$ to $2^{m-2} \cdot (R \parallel 2^{i+1-m}R)$.

In many communication systems, DDFS with quadrature (sine and cosine) outputs is desired. To implement this type of DDFS, one can use two nonlinear DACs in place of the two ROMs and the two linear DACs that are used in conventional quadrature DDFS. Even though the two ROMs can be designed to store sine values and cosine values from 0° to 45° only, two linear DACs are still needed and an extra digital multiplexer is required.

To simplify the layout and to further reduce the area requirement and the power dissipation, the two nonlinear DACs in our prototype DDFS were designed to share the same resistor string. This is achieved by wrapping around the resistor string as shown in Figure 3.5. In this case, each DAC cell has four resistors. The DAC cells are selected by the row and column decoders, which are controlled by the output bits of the complementor. The terminal nodes of the resistors are connected to four global wires through four MOSFETs as shown in Figure 3.6. When a DAC cell is selected, four voltages representing four different sine voltages with 90° phase difference can be accessed simultaneously on the four global wires. Depending on the three MSBs of the phase accumulator output, a quadrant decoder will then select two global wires

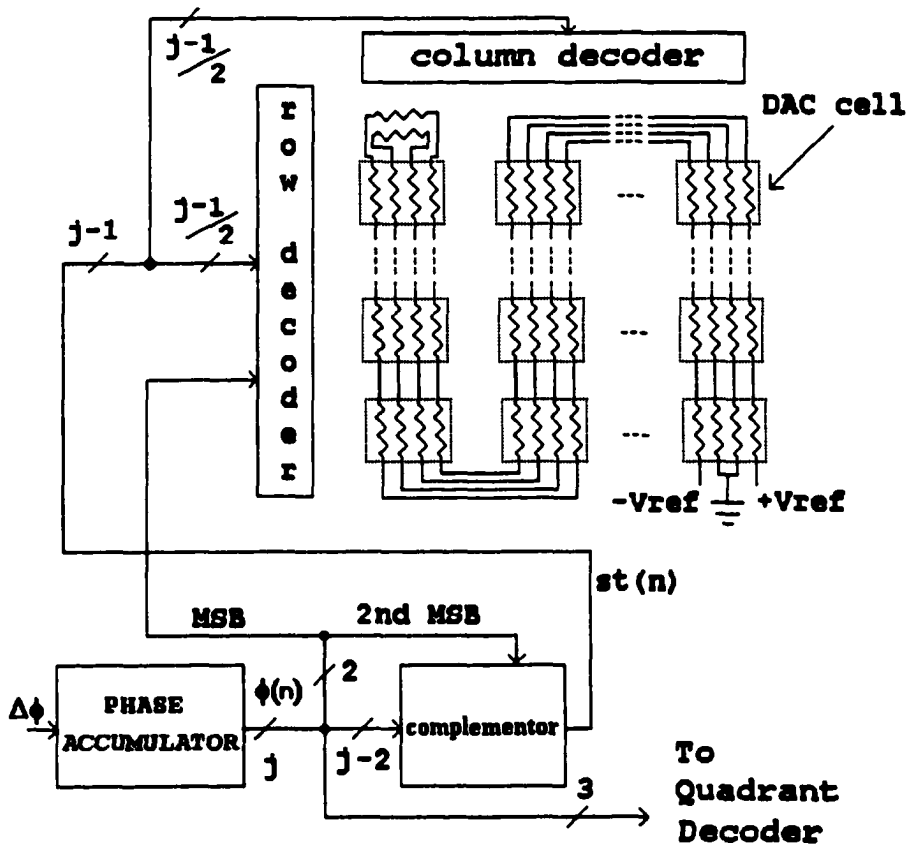



**Figure 3.5. Wrapped around resistor string DACs**

and connect them to two output buffers (Figure 3.7) so that quadrature outputs are produced. Using this scheme, the two DACs for sine and cosine outputs can share not only the resistor string but also the row and the column decoders. Consequently, the area requirement and the power dissipation can be further reduced.

Based on the above scheme, a prototype quadrature DDFS consisting of a 16-bit phase accumulator and two nonlinear DACs with 11-bit amplitude resolution (i = 10) was designed and implemented in a 1.2 μm CMOS process. The DDFS has

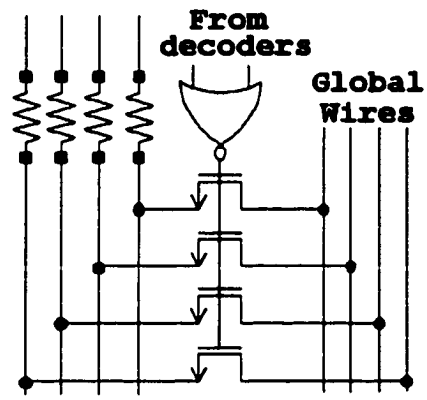



**Figure 3.6. Resistor string DAC cell design**

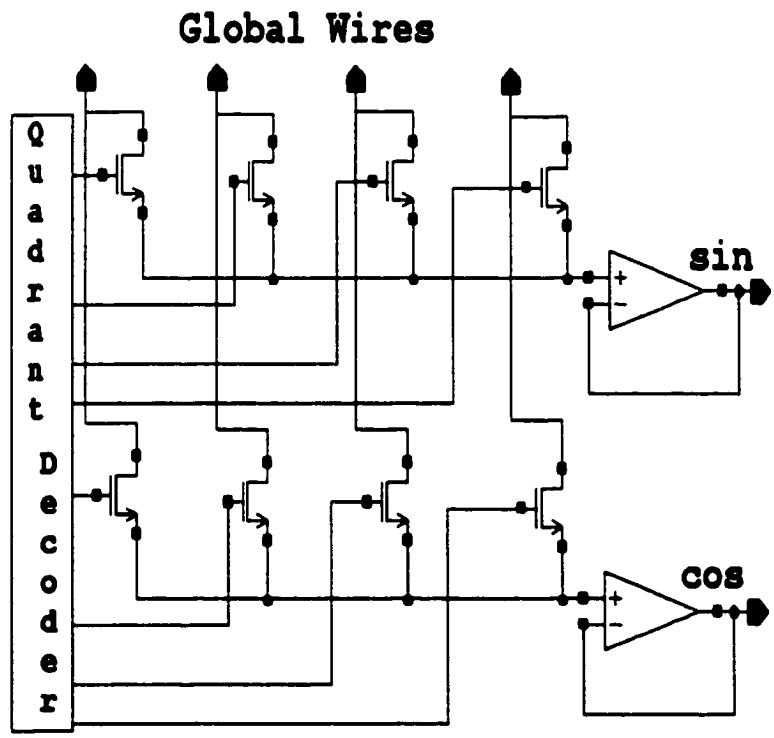



**Figure 3.7. Resistor string DAC output circuits**

10-bit phase resolution. From Table 3.1, the value of $o_{max}$ is equal to 7. Therefore, the DAC cells with an output value of $o_{max}$ have 7 unit resistors and the DAC cell size can then be determined. The resistors were implemented using polysilicon, which has a sheet resistance approximately equal to 30 Ω/square. The two analog buffers were designed based on conventional folded-cascode opamp structure. The phase accumulator was realized based on conventional carry lookahead adder using dynamic logic gates. The added low-ohmic resistor ladder with 64 resistors drops the middle node resistance from 512·R to 15.5·R, reducing the delay effects on the resistor string. The chip photo is shown in Figure 3.8. The active area is about 1.7 mm by 1.7 mm. The prototype was tested with a clock frequency of 25 MHz. In this case, the frequency resolution is equal to 381.47 Hz with a frequency switching speed of 40 ns.

The power dissipation was measured to be less than 4 mW when the supply voltage was set to 3.3 V. Most of the power is consumed by the two analog output buffers. If they are only required to drive on-chip loads, the power consumption can be further reduced. Using conventional DDFS techniques, a power dissipation of 30 to 40 mW is usually required for the same range of clock frequency [32] [23]. Figure 3.9 shows the two outputs of the DDFS for an output frequency of about 100 kHz and a peak-to-peak magnitude of about 1.5 V. The spurious free dynamic ranges (SFDRs) for two different supply voltages were measured as a function of the synthesized frequency (Figure 3.10). At low synthesized frequencies, the SFDR is about 60 dBc and 55 dBc for 4 V and 3.3 V supply, respectively. The SFDR decreases to about 20

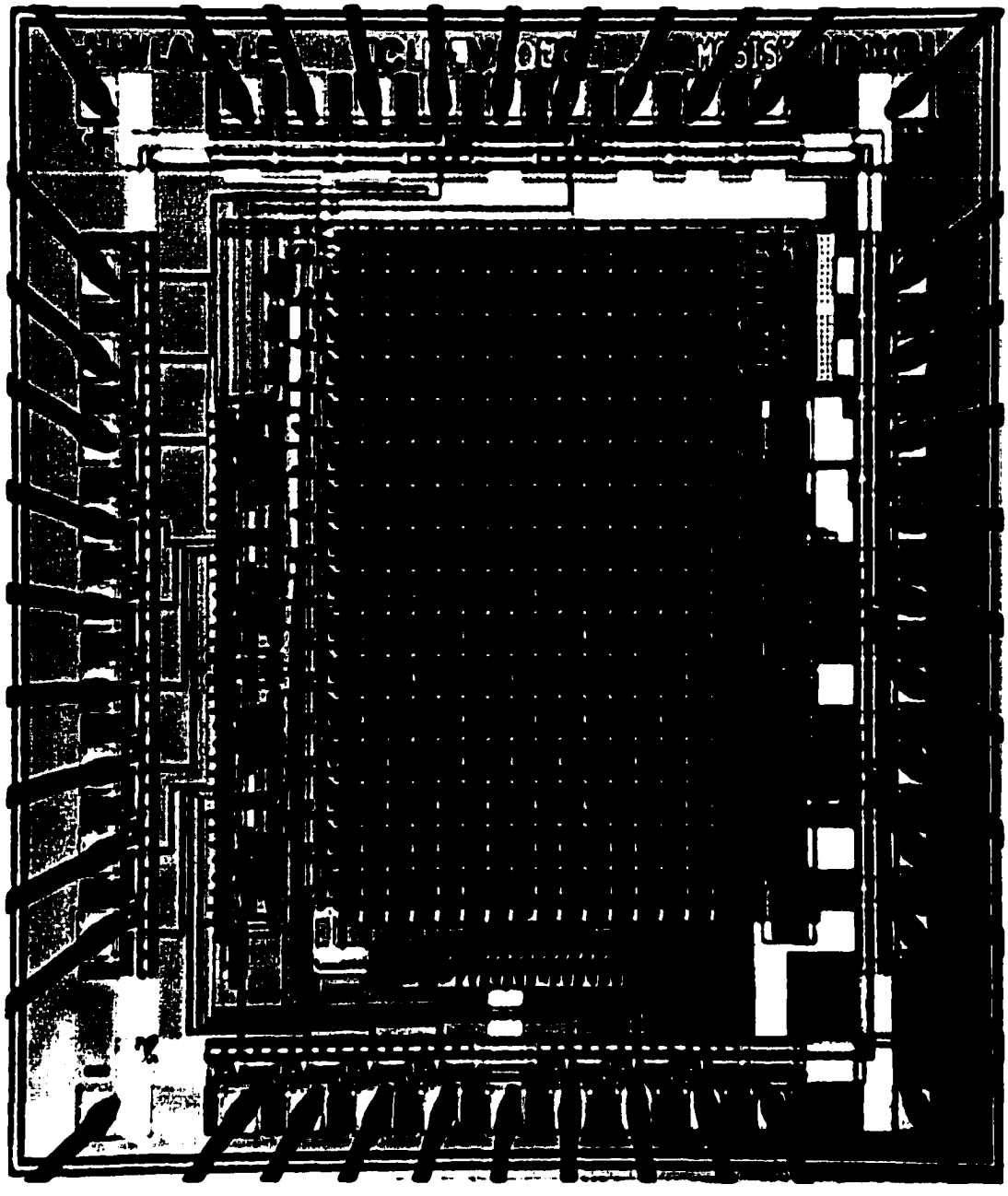


**Figure 3.8. Chip photo for the DDFS using nonlinear resistor string DACs**

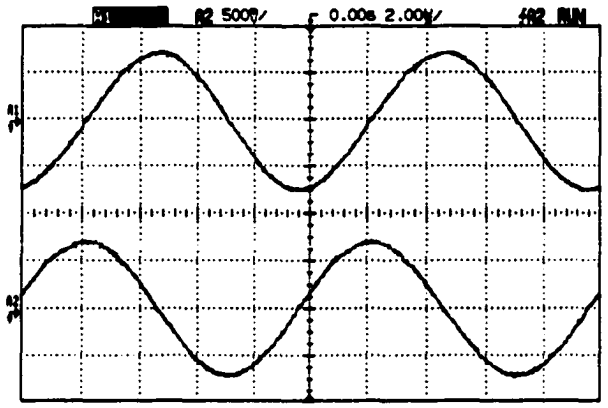


**Figure 3.9. Experimental output waveforms of the DDFS using nonlinear resistor string DACs**

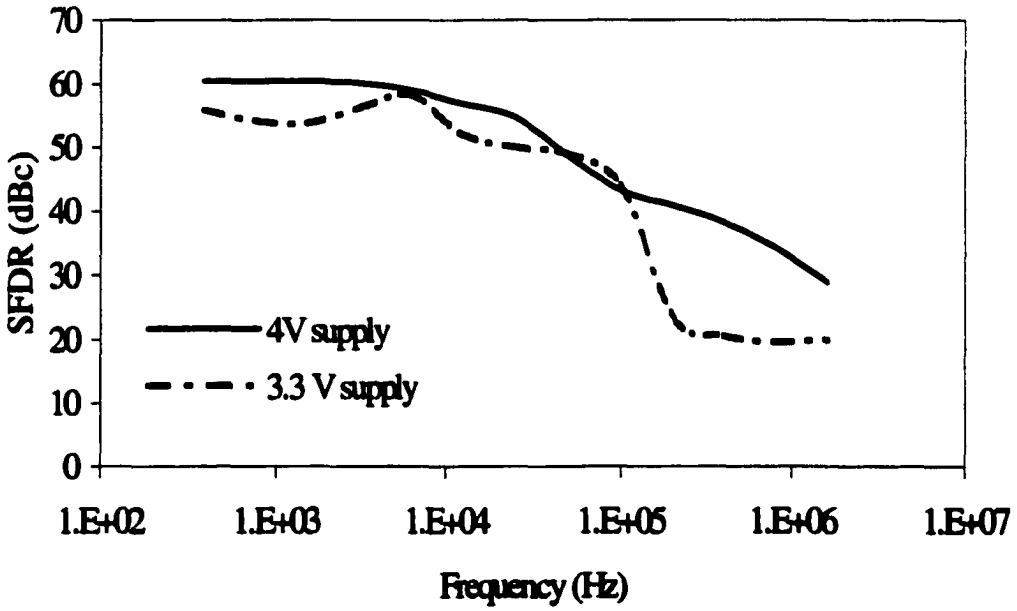



**Figure 3.10. SFDR vs. synthesized frequency for the DDFS using nonlinear resistor string DACs**

to 30 dBc for high synthesized frequencies. This is mainly due to the delay of the quadrant decoder, which generates glitches and, therefore undesired spurs when the global wires are selected and connected to the analog output buffers. These glitches can be reduced by eliminating the quadrant decoder and modifying the DAC cell design such that there is only one MOSFET switch between each node on the resistor string and the output buffers. However, it will increase the area requirement of the nonlinear DACs. The performance of the resistor string DDFS is summarized in Table 3.2.

**Table 3.2. Measured performance of resistor string DDFS**

| | |
|---|---|
| Technology | 1.2 μm CMOS |
| Clock frequency | 25 MHz |
| Phase resolution | 10 bits |
| Amplitude resolution | 11 bits |
| SFDR | 60 dBc @ 4 V<br>55 dBc @ 3.3 V |
| Power dissipation | 4 mW @ 3.3 V |
| Active Area | 1.7 mm by 1.7 mm |

## 3.6 Quadrature DDFS Using Nonlinear Current-Mode DACs

Another approach to realize the nonlinear DAC is to use current-mode techniques. This approach is similar to the design of a conventional linear DAC based on current-cell matrix configuration (RAMDAC) [20]. Each DAC cell is required to output a current proportional to $o_k$ and the sine wave output is obtained by summing the output currents from cell 0 to cell st(n). When compared to the design of an i-bit linear RAMDAC, the nonlinear DAC will dissipate approximately the same amount of power since they both require the same number of total current sources.

A prototype quadrature DDFS was designed using this technique. The architecture is shown in Figure 3.11. It consists of a 14-bit phase accumulator and two nonlinear DACs with an amplitude resolution of 11 bits (i = 10). The phase resolution for this design is also 10 bits. The two nonlinear DACs share the same row thermometer code decoder and column thermometer code decoder. Each DAC cell has two current outputs that are connected to the corresponding outputs of other cells. The sums of the DAC cells' current outputs are converted to quadrature output voltages by two off-chip resistors. The detail design of each DAC cell is shown in Figure 3.12. Each DAC cell consists of two sets of current switches, which are used to produce the sine output and the cosine output, respectively. For the sine output, two current-steering pairs (P and N) are connected to two tail currents, which are both proportional to $o_k$. The P pair and N pair are used for producing the positive and negative regions of the sine wave output, respectively. For the positive region, the

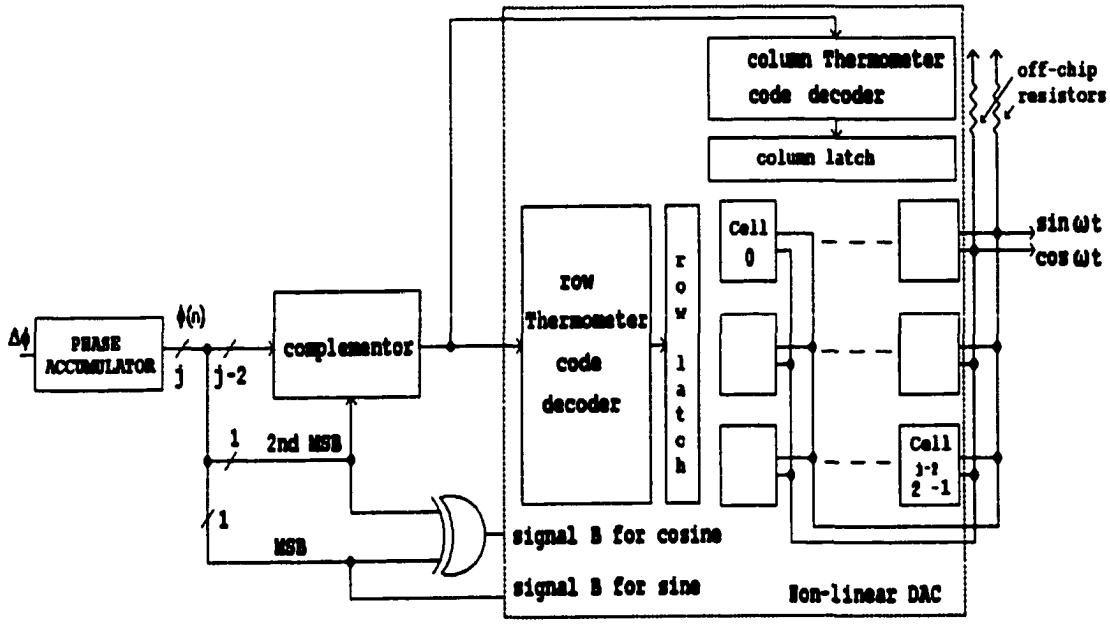



**Figure 3.11. Architecture of the quadrature DDFS using nonlinear current-mode DACs**

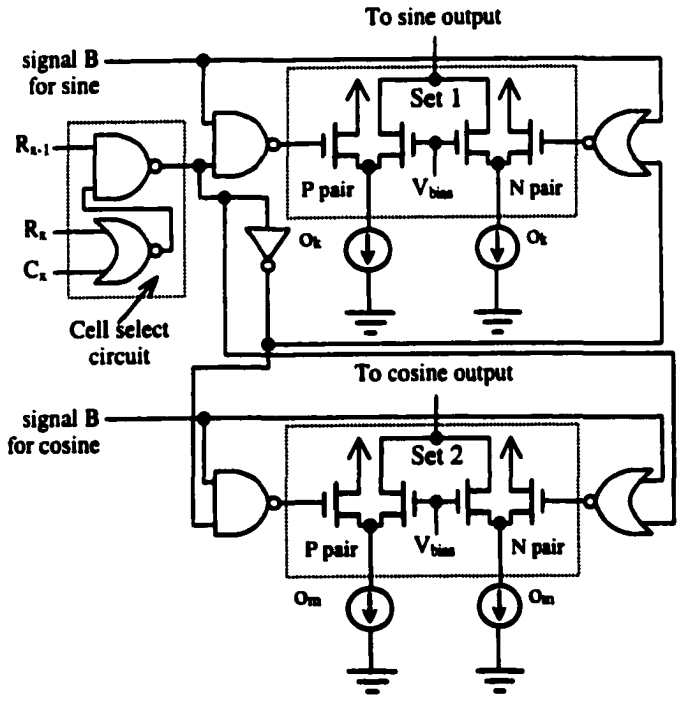



**Figure 3.12. The detail design of each DAC cell**

signal B for the sine output will turn high, and the N pairs in all the DAC cells that are connected to the sine output will be on. The thermometer code decoders will turn on the P pairs according to st(n). For the negative region, the signal B will turn low and all the P pairs are off. The thermometer code will turn on the N pairs according to st(n). This scheme will ensure that the transition between the positive and the negative region changes monotonically and hence, the output will have low glitching noise. Signal B for the current steering pairs of the sine output is connected to the $\overline{MSB}$ of the phase accumulator output. The same thermometer code decoders are used to control the current-steering pairs for both sine and cosine outputs. However, the cell select circuit outputs that are connected to the current-steering pairs for the cosine output are inverted, and the tail currents of the cosine output for the k-th cell are proportional to $o_m$ where m is equal to $2^{j-2} - 1 - k$ . According to this arrangement, in the first quadrant, the cosine output decreases while the sine output increases for increasing st(n). To obtain different quadrants for the cosine output, both the MSB and the second MSB of the phase accumulator output are used to determine the signal B for the cosine output (Figures 3.11 and 3.12). Using this scheme, the two nonlinear DACs are combined and share the same thermometer code decoders. As a result, the power dissipation and the die area are minimized.

A simplified diagram for the phase accumulator is shown in Figure 3.13. It consists of a 14-bit adder and a 14-bit register, which contains two 14-bit dynamic D-latches latched at clk and $\overline{clk}$ . The adder was designed based on the carry

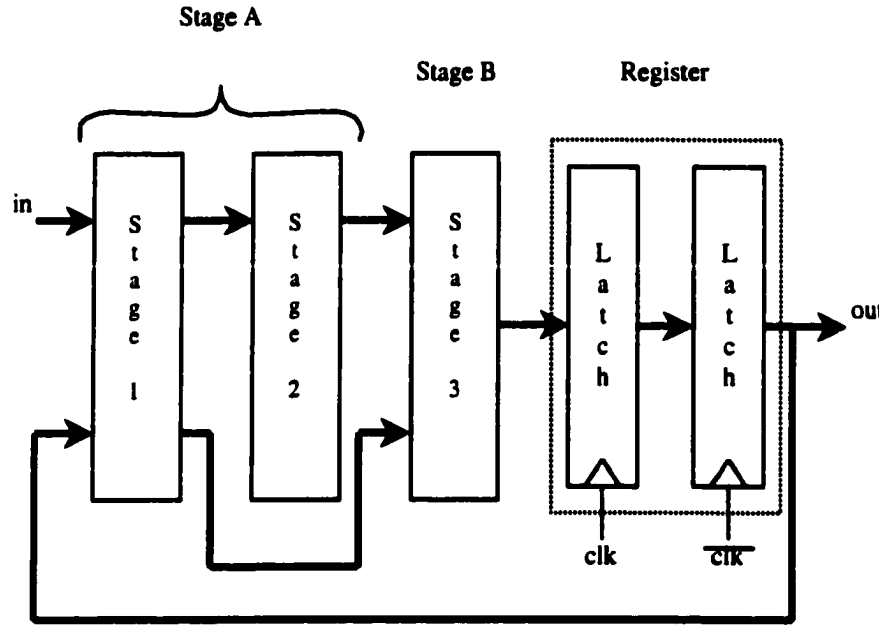



**Figure 3.13. Simplified phase accumulator design for the DDFS using nonlinear current-mode DACs**

lookahead technique proposed in [33]. This technique utilizes enhanced multiple output domino logic (EMODL) gates to implement group generates and group propagates (stage 1), carry chain generation (stage 2), and sum generation (stage 3). Using this technique, low-power and high-speed adders can be realized [33]. Each stage of the adder has a number of EMODL gates working in parallel. Hence, the delay in each stage is equivalent to the delay of one EMODL gate delay. Since all three stages are in cascade and the evaluation phase of these stages has to be finished in half of a clock period, the required clock period is too long to achieve high clock frequency. To reduce the clock period, the first 14-bit D-latch in the 14-bit register is moved between stage 2 and stage 3 (Figure 3.13). Stage 1 and stage 2 are combined

and considered as stage A. Stage 3 is then referred to as stage B. Stage A is designed to precharge when clk is low and evaluate when clk is high. Stage B is designed to operate exactly at the opposite clock phases. When stage A is precharging, stage B is evaluating and vice versa. Hence, the entire clock cycle can be utilized for evaluation and the clock period is shortened by about 30%. Figure 3.14 shows the detail design of the phase accumulator where $a_1$ to $a_{14}$ represent the phase accumulator input bits and $b_1$ to $b_{14}$ represent the phase accumulator output bits. The signals $g_i$'s, $p_i$'s and $x_i$'s are the generate signals ($a_i \cdot b_i$), the propagate signals ($a_i + b_i$), and the exclusive-OR signals ($a_i \oplus b_i$), respectively. The signals $g_i$'s and $p_i$'s with a symbol $\wedge$ on top, represent the pseudocompliments of the generate signals ($\overline{a_i} \cdot \overline{b_i}$) and the propagate signals ($\overline{a_i} + \overline{b_i}$) [33]. The sum bits $s_i$'s (i.e. $b_i$'s) are computed by combining the carry outputs ($c_0$, $c_4$, $c_8$ and $c_{12}$), the exclusive-OR signals ($x_1$ to $x_{14}$), the generate signals ($g_1$ to $g_{13}$) and their pseudocompliments. The carry outputs are obtained from the group generates $g_{i,j}$'s and the group propagates $p_{i,j}$'s and their pseudocompliments. The design of the EMODL gate for generating the output sums $s_1$ to $s_4$ is illustrated in Figure 3.15. The prototype DDFS was designed and implemented in a 0.5 μm CMOS process. The chip photo is shown in Figure 3.16. The active area is about 1.0 mm by 1.6 mm. The design was tested at a clock frequency $f_{clk}$ of 230 MHz. The frequency resolution at this clock frequency is equal to 14.04 kHz with the frequency switching speed of 9.1 ns. For clock frequency higher than 250 MHz, the DDFS no longer produced sine waves at the outputs due to internal timing limitation of the phase

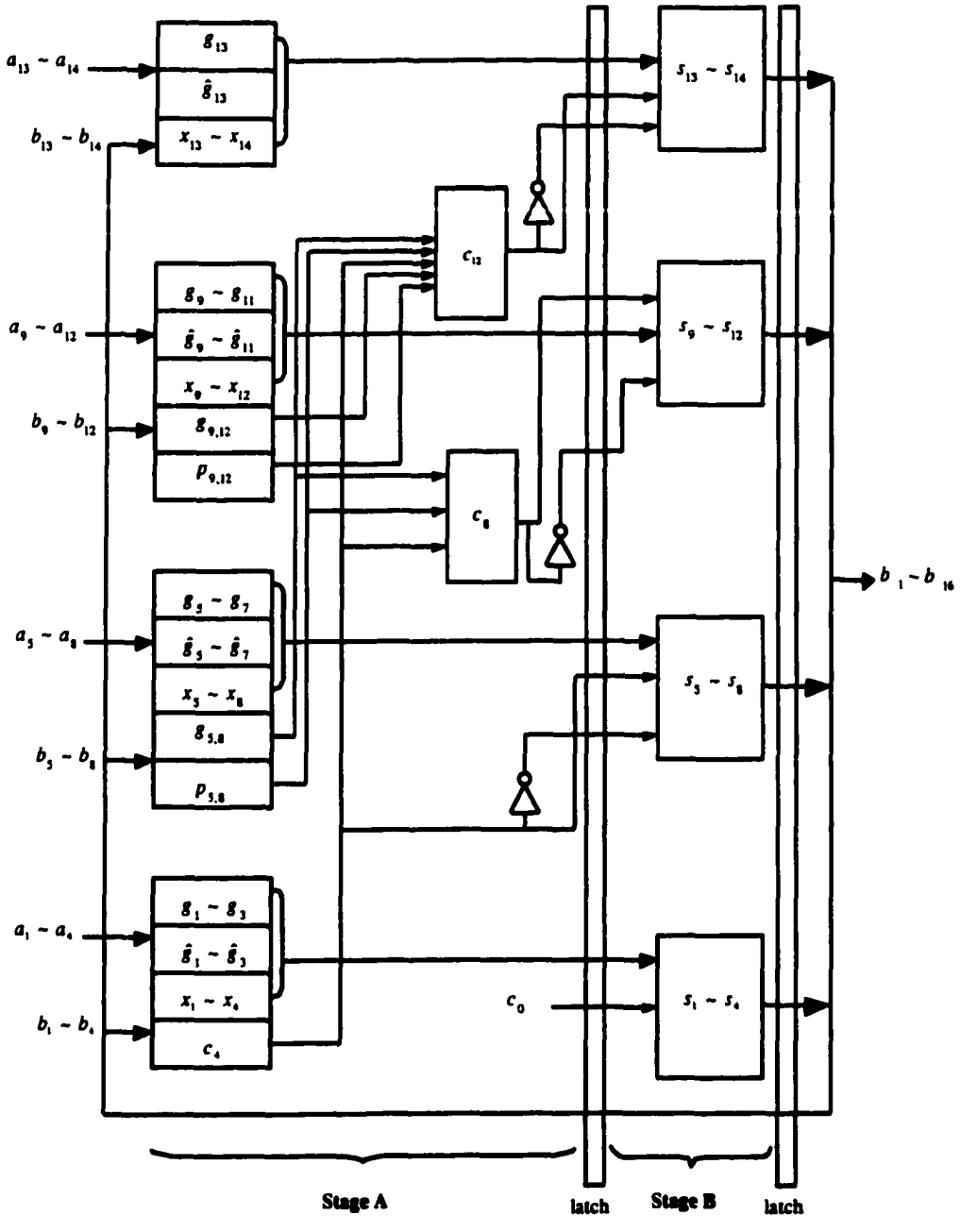



**Figure 3.14. Detail diagram for the 14-bit phase accumulator**

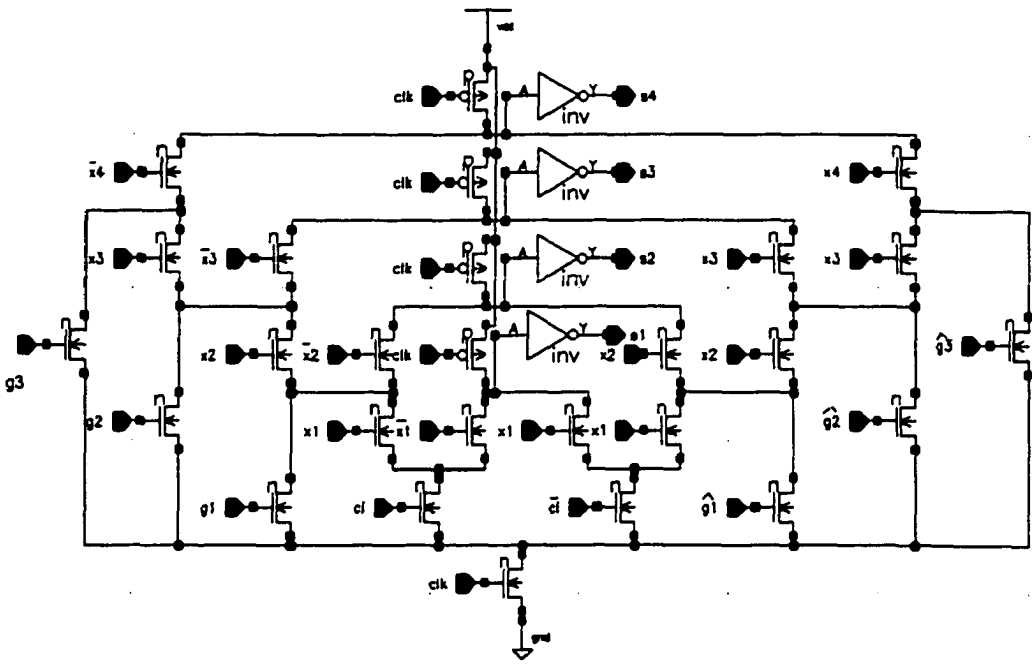



**Figure 3.15. EMODL gate for generating the output sums $s_1$ to $s_4$**

accumulator. Figure 3.17 shows the two outputs of the DDFS for an output frequency of 1.8 MHz. These outputs were produced using two off-chip 50 Ω resistors. The peak-to-peak magnitudes were about 350 mV. The total power dissipation was measured to be 92 mW for a 3.3 V power supply, $f_{clk}$ = 230 MHz and a synthesized frequency of 1.8 MHz. The phase accumulator dissipates approximately 22 mW. Figures 3.18a and 3.18b show the output spectra for output frequencies set at 120 kHz and 7.2 MHz, respectively. The clock frequency $f_{clk}$ was set at 230 MHz. The SFDR vs. synthesized frequency was measured as shown in Figure 3.19a. The SFDR is better than 55 dBc at low synthesized frequencies. The SFDR degrades at high-synthesized frequencies. This is mainly due to switching feedthrough from the digital

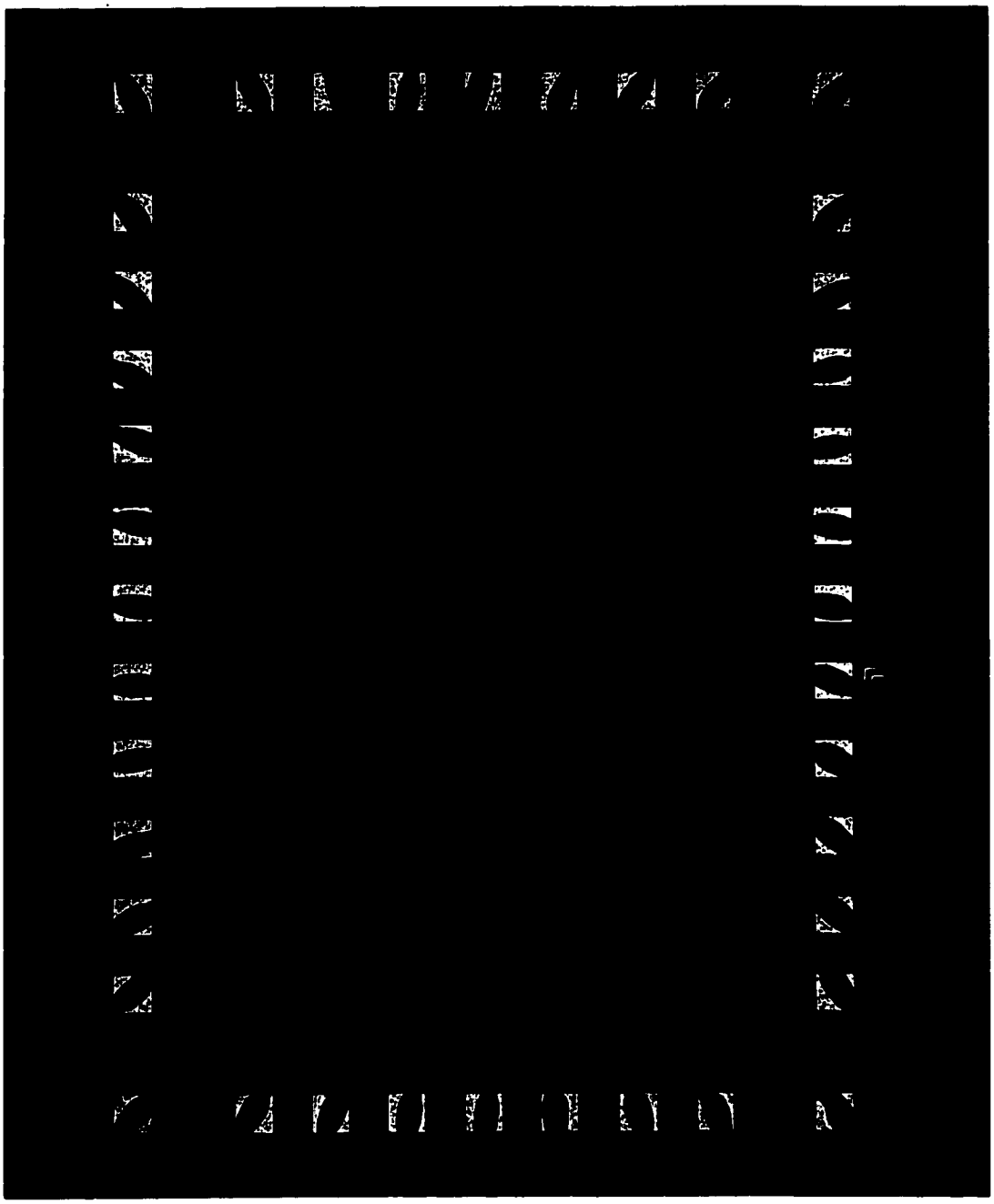


**Figure 3.16. Chip photo for the DDFS using nonlinear current-mode DACs**

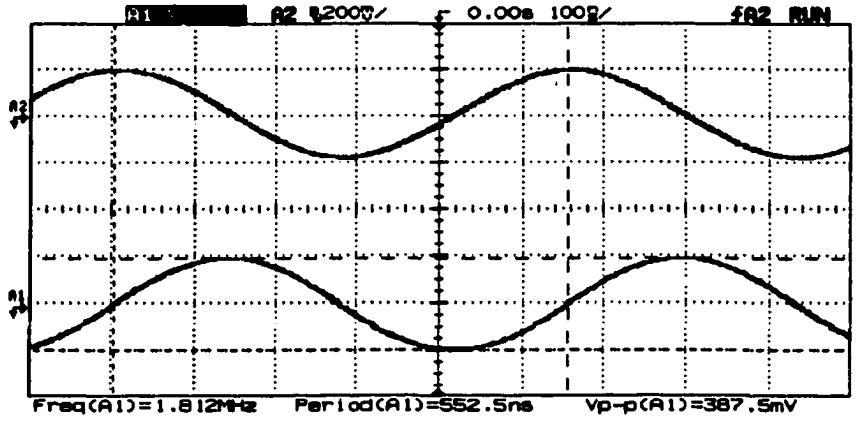
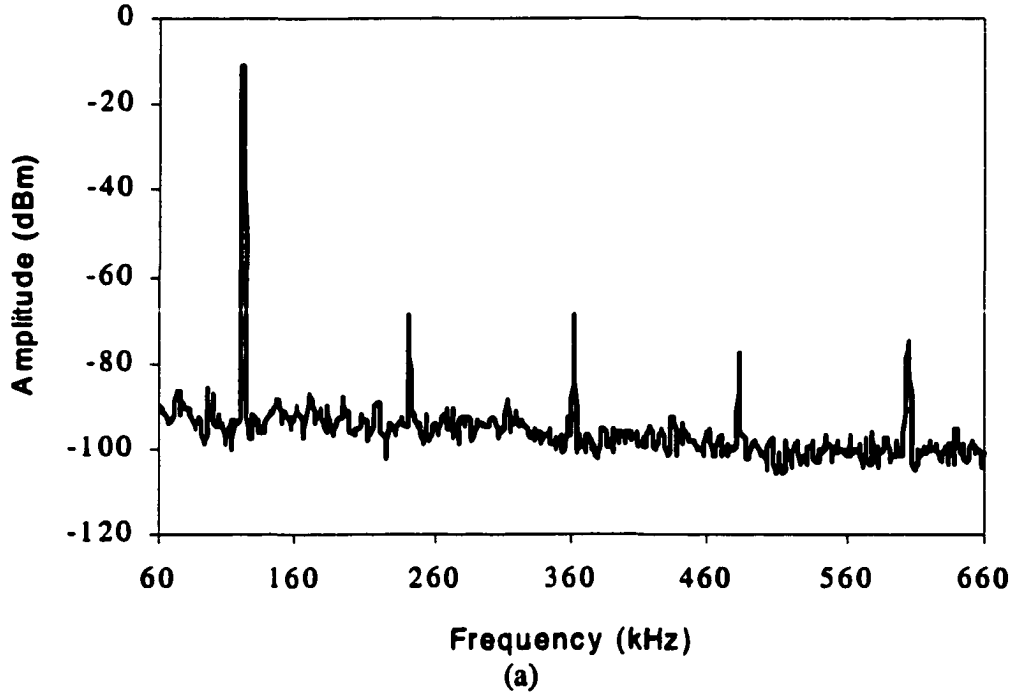



**Figure 3.17. Experimental output waveforms for the DDFS using nonlinear current-mode DACs**

inputs of the current-steering pairs to the biasing voltage of the current sources. As a result, undesired harmonics and other spurious signals were generated. A better result can be obtained if an on-chip biasing source with low output impedance is used. Further improvements can be obtained if latches are used inside each DAC cell to synchronize the digital inputs of the current-steering pairs.

For synthesized frequency of $1/64f_{clk}$, the SFDR vs. clock frequency was also measured as shown in Figure 3.19b. The power dissipation vs. clock frequency and vs. synthesized frequency is shown in Figures 3.20a and 3.20b, respectively.

Table 3.3 shows a comparison between different recently reported DDFSs that are operated at the same range of clock frequency (100 - 200 MHz). Notice that two of the reported DDFSs do not provide quadrature outputs and two of them do not have on-chip DACs for converting the quantized sine waves to analog outputs. The proposed design dissipates significantly less power (more than three times less) than



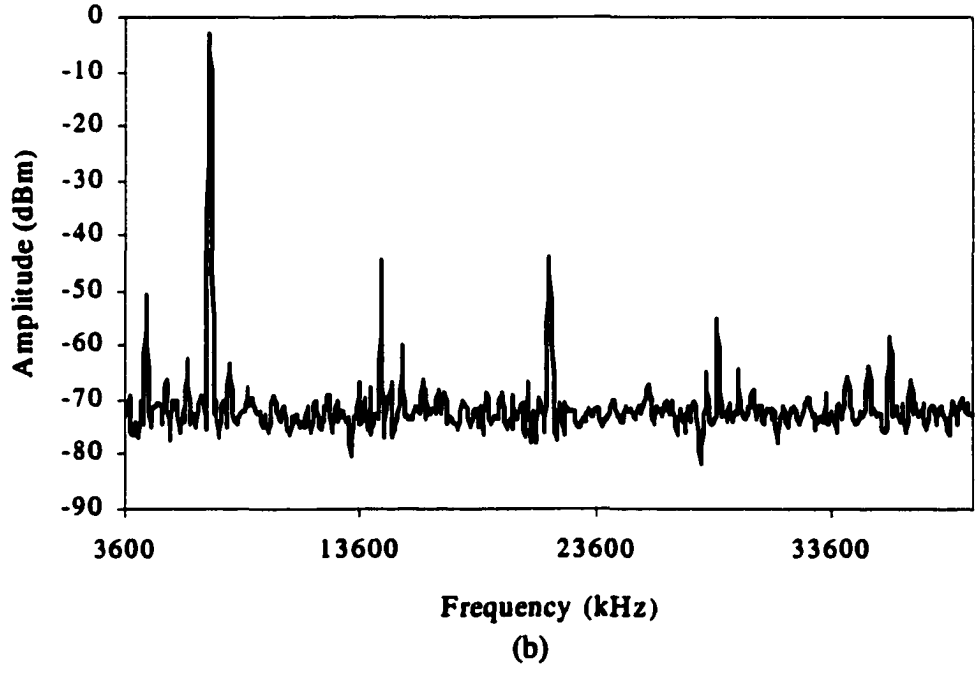




**Figure 3.18. Spectrum plots of the output at 230 MHz clock frequency (a) 120 kHz synthesized frequency and (b) 7.2 MHz synthesized frequency**

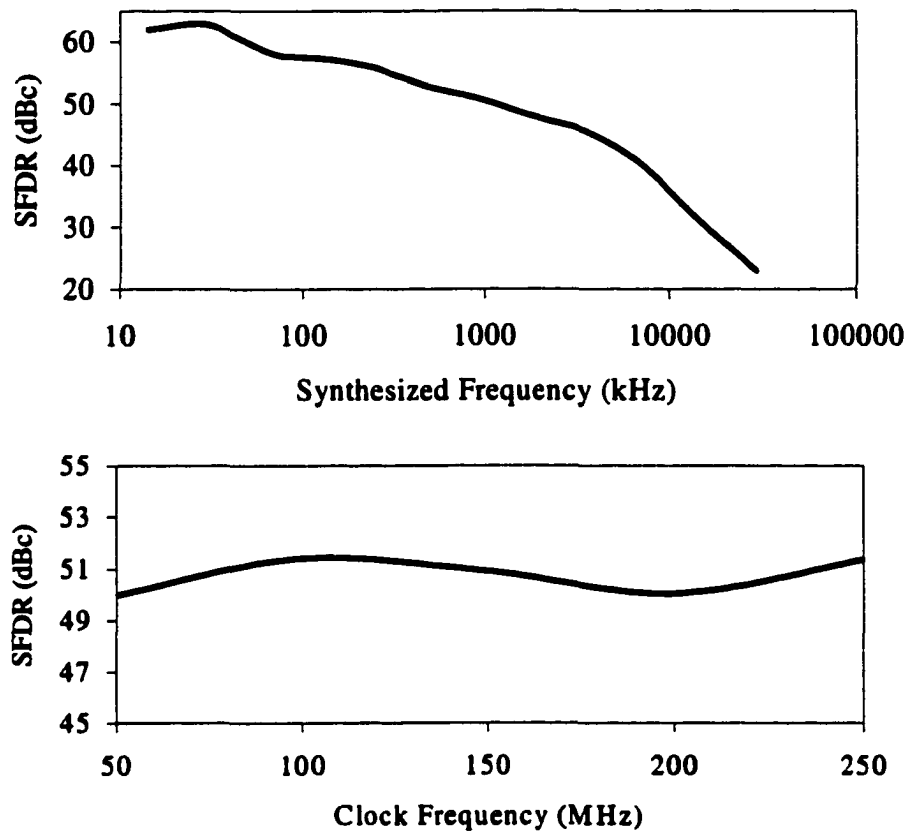



**Figure 3.19. SFDR vs. (a) synthesized frequency at a clock frequency of 230 MHz and (b) clock frequency for synthesized frequency of $1/64f_{clk}$**

others do. This is achieved due mainly to the use of nonlinear DACs in place of the ROM lookup tables, other logic circuits, and the linear DACs in a conventional DDFS.

## 3.7 Summary

In this chapter, a new design technique for DDFS using nonlinear DACs is proposed. Compared to conventional ROM based DDFS, it requires significantly less

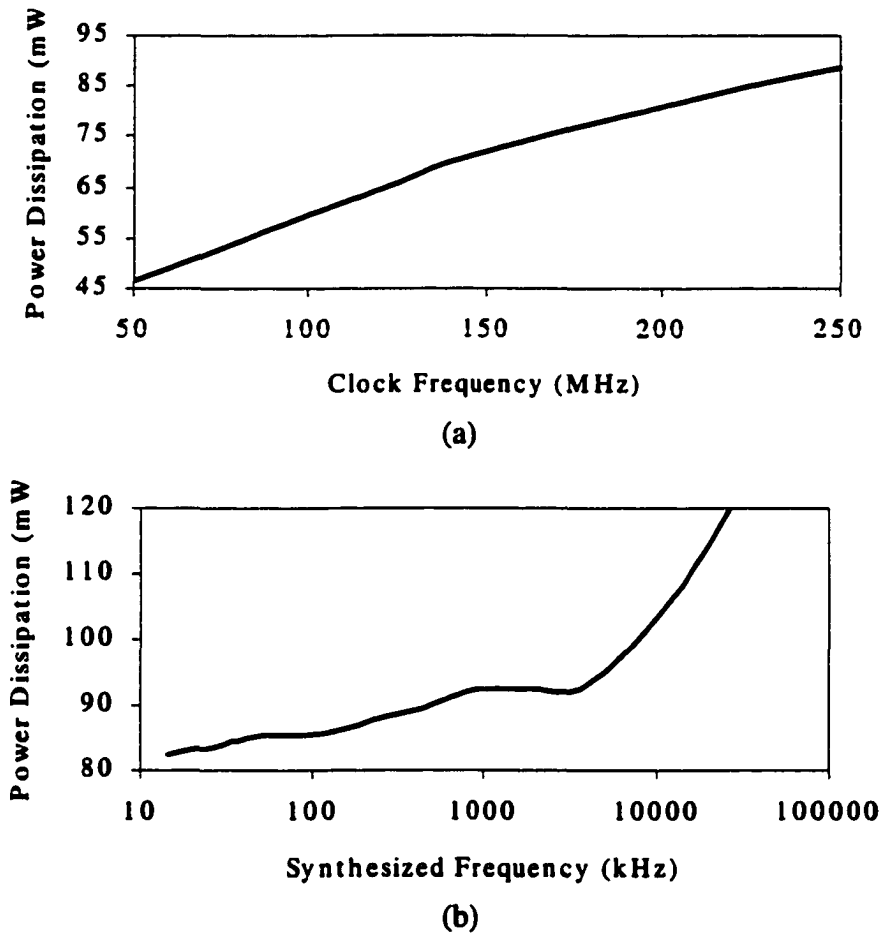



**Figure 3.20. Power dissipation vs. clock frequency for (a) synthesized frequency of $1/64f_{clk}$ and (b) synthesized frequency at a clock frequency of 230 MHz**

power. The nonlinear DACs can be designed using conventional thermometer code DAC design techniques, including the use of resistor string and current-mode approaches. It is also possible to implement the nonlinear DACs based on switched-capacitor techniques. The only difference from the conventional linear DAC design is that each DAC cell will have a different number of resistors, capacitors or current sources. For a given phase resolution and magnitude resolution requirement, the

**Table 3.3. Comparison between different recently reported DDFSs**

| | [34] | [35]† | [36] | [37] | This work†† |
|---|---|---|---|---|---|
| Technology | 1.25 μm CMOS | 0.8 μm CMOS | 0.8 μm BiCMOS | 0.5 μm CMOS | 0.5 μm CMOS |
| Clock frequency | 150 MHz | 200 MHz | 110 MHz | 150 MHz | 230 MHz |
| Phase resolution | 15 bits | 14 bits | 12 bits | 12 bits | 10 bits |
| Amplitude resolution | 12 bits | 12 bits | 10 bits | 10 bits | 11 bits |
| On-chip DACs | No | No | Yes | Yes | Yes |
| Quadrature outputs | No | Yes | No | Yes | Yes |
| Power dissipation | 1 W @ 5V | 2 W @ 5V | 282 mW @ 3.3 V | 496 mW @ 3.3 V | 92 mW @ 3.3 V |
| Active Area | ≈ 16 $mm^2$ | 15.9 $mm^2$ | 3.9 $mm^2$ | 9 $mm^2$ | 1.6 $mm^2$ |

† Including four 12-bit digital multipliers for quadrature amplitude modulation
†† Using current-mode nonlinear DACs

number of DAC cells and the output values of the DAC cells can be determined using the DAC design procedure outlined in this chapter. Furthermore, as discussed in section 3.4, the proposed technique will have significant advantages in terms of power dissipation and die area over conventional ROM based DDFSs for high phase

resolutions. The only drawback for the proposed technique is that digital amplitude modulation cannot be incorporated into the DDFS easily. Nevertheless, amplitude modulation can be achieved using other means, for example, using analog mixers.

To demonstrate the proposed technique, two quadrature DDFSs, one implemented using resistor string and the other implemented using current sources, are described in this chapter. The SFDRs for these two DDFSs were measured to be over 55 dBc at low synthesized frequencies with frequency switching speeds of 40 ns and 9.1 ns, respectively. At 3.3 V, they consume 4 mW and 92 mW for a clock frequency of 25 MHz and 230 MHz, respectively. For low clock frequency and low power applications such as for instrumentation, the DDFS based on nonlinear resistor string is preferable. The current-mode approach is more suitable for high frequency applications. Compared to conventional ROM based DDFSs, the proposed design technique for DDFSs require significantly less power dissipation and, therefore, can be used in portable wireless communication systems.

# CHAPTER 4. LOW VOLTAGE DATA CONVERTER DESIGN

Increasing demand for portable equipment in all market segments and the reduction of IC supply voltage due to technology scaling force the need to find circuit techniques that can operate at power supply voltages in the range of 1 to 2 V, with low power consumption. It is possible to operate digital circuits at such low voltage using technologies that are available today [38] and the only drawback is the increase in delay time. However, scaling the supply voltage down presents a formidable challenge to design analog circuits. This challenge comes from the fact that the threshold voltages of MOSFET devices are relatively high for the given supply voltage ranges. For future standard CMOS processes, the threshold voltages may not decrease much below what is available today [39]. Although low voltage analog circuit design can be achieved using low threshold voltage devices [40] [41], it is a high-cost solution due to the requirement of non-standard processing. Another solution is to use on-chip DC-to-DC converters or other bootstrapping techniques to increase the internal supply voltage. However, high internal supply voltage may not be tolerable for scaled-down technologies. Therefore, circuit techniques must be developed to operate analog circuits at a low supply voltage using relatively high

threshold voltage devices. It should be noted that these techniques will offer the potential for the best utilization of a given technology at any voltage range even if low threshold voltage technologies become standard. In this chapter we present an alternative low voltage analog circuit design technique and use this technique to implement a 10-bit DAC and an 8-bit successive approximation ADC to operate at 1 V supply voltage.

## 4.1 Introduction

In many mixed-mode applications, digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) are required for interfacing analog and digital circuits. These data converters are usually necessary to be integrated with complex digital signal processor (DSP) in a low-cost CMOS technology. However, due to low supply voltage of DSP circuits, data converters that are integrated with a DSP are forced to operate in the same range of supply voltage. As we mentioned before, designing data converter circuits operating at low supply voltage presents a great challenge. In this section we discuss some of these challenges and propose techniques to overcome them.

### 4.1.1 Challenges in designing low voltage DAC

One of the most common building blocks in data converter circuit design is the opamp. To achieve low supply voltages with rail-to-rail signal swings, opamp

input stages with rail-to-rail input common-mode ranges have been developed [42] [43] [44] in standard CMOS process with a supply voltage in the range of 1.2 V to 3 V. Supply voltage can go as low as 1 V if the input differential stage of an opamp is realized using bulk driven MOSFETs [45] or depletion devices available in some specialized BiCMOS process [46]. However, designing analog circuits that require switches such as sample-and-hold amplifiers at low supply voltages still remains a challenge. When the supply voltage is less than the sum of the threshold voltages of PMOS and NMOS, the switches will fail to pass voltages in the mid-range of the power supply even if transmission gates are used [47]. To deal with this problem, switched-opamp technique has been proposed [48]. This technique avoids the use of critical switches to pass voltages in the mid-range by turning on or off the opamps, and hence, it can be used effectively whenever the output of an opamp drives the capacitors connected to the inputs of another opamps. However, there are two disadvantages in this technique. First, at the front end, critical switches connected to off-chip input signals cannot be avoided and direct input through MOSFET switches usually result in a low signal input range [47] [49]. Furthermore, the outputs of the opamps in a switched-opamp circuit are always required to swing from one of the supply voltage during one of the clock phases and hence, the output signals may be slew rate limited. Despite these disadvantages, switched-opamp technique is a very effective technique to implement low voltage discrete-time analog circuits. Many

switched-capacitor circuits can be implemented using switched-opamp technique such as discrete-time filter [47] and sigma-delta modulator [50].

### 4.1.2 The proposed technique

In this chapter, an alternative low voltage analog circuit design technique is presented. Similar to switched-opamp technique, it avoids the need for a wide common-mode input range opamp. At the same time, no critical switches for passing voltage signals are needed. Using the proposed technique, a 10-bit DAC and an 8-bit successive approximation ADC were implemented in a conventional 1.2 μm CMOS process with $V_{tn} \approx 0.7$ V and $V_{tp} \approx -0.8$ V. Both converters use 1 V supply voltage. Low-voltage S/H and DAC with large signal swing are realized based on inverting opamp configurations with biasing currents added to the opamp negative input terminal so that the opamp input common-mode voltages can be biased near ground to minimize the required supply voltage. At the same time, the input and output quiescent voltages can be set at the middle of the supply rails for maximum signal swing. This is achieved by introducing a current source or a resistor between the opamp negative input terminal and one of the supply rails. Hence, opamps with limited input common-mode range can be used in this technique. In addition, switches can be incorporated in these circuits to allow a wide range of applications. This technique also allows large input and output signal swings (close to rail-to-rail) even at a very low voltage supply. For ADCs, comparator is usually required. Low-voltage

latched comparator is realized based on current-mode approach. The DAC and ADC have been tested at a 1 V supply. The 10-bit DAC consumes less than 0.45 mW at 1 MS/s sampling rate and has a maximum throughput of 1 MS/s with close to rail-to-rail output (0.1 V to 0.9 V). The maximum DNL and INL were measured to be 1.7 LSBs and 3.0 LSBs, respectively. The entire 8-bit ADC including the digital circuits consumes less than 0.34 mW at 1 V supply. The effective number of bits for a 1 kHz, 850 mV peak-to-peak input signal is 7.9 bits. This ADC is designed for medium quality voice and audio applications.

## 4.2 10-bit Digital-to-Analog Converter

To demonstrate the proposed technique, we first introduce the biased inverting opamp configuration for low voltage applications. We also present possible ways to solve the switch problem in low voltage designs by avoiding critical voltage switches. Then, a possible biasing current generation circuit will follow and finally, the complete 10-bit DAC design will be presented.

### 4.2.1 Biased inverting opamp

Figure 4.1 illustrates a conventional CMOS opamp input stage utilizing a PMOS differential pair. The maximum input common-mode voltage is limited to $V_{DD}$ - 2 $V_{SDsat}$ - $|V_{tp}|$. For a conventional inverting opamp circuit, which has a structure similar to that shown in Figure 4.2a, but without the current source $I_B$, the

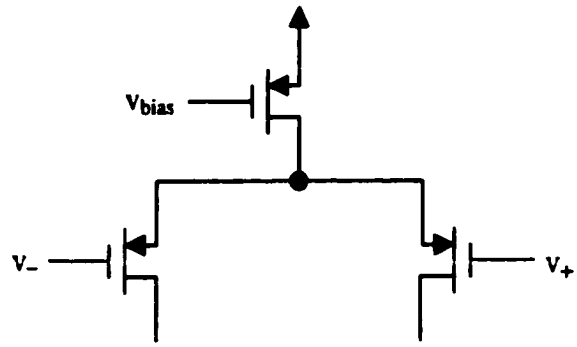



**Figure 4.1. A PMOS differential input stage**

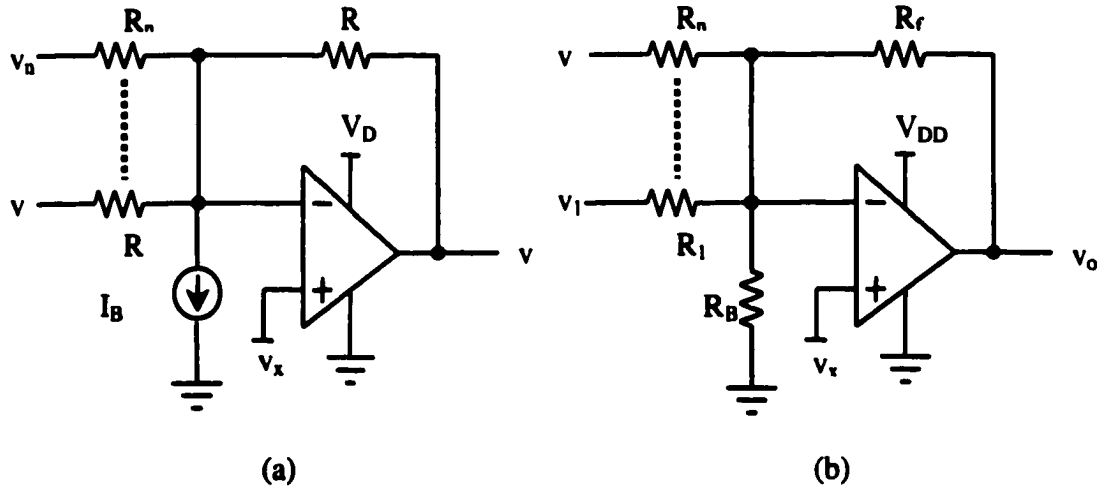



**Figure 4.2. Proposed biasing schemes that use (a) a current source and (b) a resistor**

input/output quiescent voltage and the opamp input common-mode voltage $v_x$ are normally set to $V_{DD}/2$ in order to maximize the signal swing. Due to the limited opamp input common-mode range, the supply voltage is required to be greater than $2 \times (2\ V_{SDsat} + |V_{tp}|)$. Therefore, the circuit cannot operate at 1 V supply for $|V_{tp}|$

greater than 0.4 V. To reduce the supply voltage requirement, the opamp input common-mode voltage $v_x$ has to be biased to a voltage close to ground, independent of the input and output quiescent voltage. To achieve this goal, we propose a simple technique that may have been known for years but has not been applied effectively to the design of low voltage analog circuits. In this technique, a current source $I_B$ is introduced as shown in Figure 4.2a. If the input and output quiescent voltages are equal to $V_{DD}/2$, the required value for $I_B$ can be determined as:

$$I_B = \left( \frac{V_{DD}}{2} - v_x \right) \left( \frac{1}{R_f} + \frac{1}{R_1 // \Lambda // R_n} \right) \qquad (4.1)$$

Since $I_B$ is most conveniently realized using an NMOS, the value of $v_X$ has to be greater than $V_{DSsat}$ and hence, the minimum supply voltage for the circuit is $V_{DSsat} + 2\,V_{SDsat} + |V_{tp}|$. Without the addition of the current source, the minimum supply voltage has to be approximately doubled. If the input stage of the opamp is realized using NMOS differential pair, setting $v_x$ close to $V_{DD}$ with a PMOS current source $I_B$ connected between the opamp negative input terminal and $V_{DD}$ will minimize the supply voltage.

Based on the same principle, another approach to bias the opamp input common-mode voltage is to use a resistor or a MOSFET operating in triode region as shown in Figure 4.2b. The resistance $R_B$ can be determined as:

$$R_B = \frac{v_x}{\frac{V_{DD}}{2} - v_x} (R_f // R_1 // \Lambda // R_n) \qquad (4.2)$$

The second approach has an advantage of setting $v_x$ to a value lower than one $V_{DSsat}$ (but greater than ground). Both approaches can also be extended to convert a fully differential inverting opamp configuration into a low voltage design. In this case, two current sources or two resistors are required to connect to the fully differential opamp inputs, and the values of the current sources or the values of the resistors can be determined based on the input and output common-mode voltages.

Addition of the current source or the resistor will induce minimal effects on the low frequency AC response since they are connected to the virtual ground of the opamp. However, at high frequency, the bandwidths of the two schemes are different. The feedback factor $\beta_i$ for the biasing scheme that uses current source can be determined as,

$$\beta_i = \frac{R_1 // \Lambda // R_n // r_{ds}}{R_1 // \Lambda // R_n // r_{ds} + R_f} \qquad (4.3)$$

where $r_{ds}$ is the output resistance of the current source. The feedback factor $\beta_r$ for the resistor scheme can also be expressed similar to equation 4.3 with $r_{ds}$ changed to $R_B$. As observed from equation 4.2, $R_B$ is usually smaller than $R_1//\cdots//R_n$ and $r_{ds}$. Thus $\beta_i$ will be larger than $\beta_r$ and therefore, the scheme that uses current source will have a higher bandwidth given by $\beta_I.f_t$ where $f_t$ is the unity gain frequency of the opamp. The proposed biasing schemes can be used to convert any circuit that uses inverting opamp configuration such as continuous time active RC filters into a low voltage design with a minimum supply voltage approximately equal to $3\ V_{DSsat} + V_t$.

The proposed technique can also be used for interfacing circuits that require higher supply voltage. This is possible since there is no limit on the voltage range at the input of the resistor except the limit posed by the input protection diodes in the ESD structure. However, these diodes can be omitted if necessary. To keep the quiescent output voltage at $V_{DD}/2$, proper values for the current source $I_B$ or the resistor $R_B$ need to be re-determined for the new quiescent input voltage.

The design of the opamps that we used in the DAC is shown in Figure 4.3. It is a two-stage architecture that consists of a PMOS differential pair, a low voltage current mirror and a common source second stage as discussed in [51]. The output

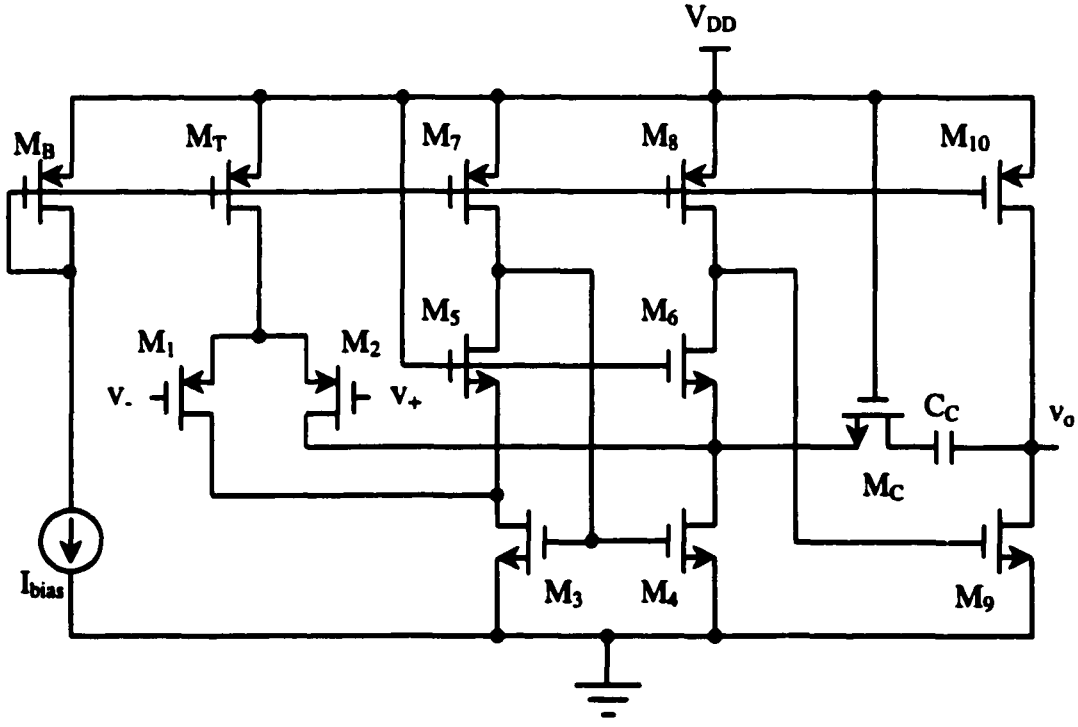



**Figure 4.3. Single-ended 1V opamp design**

voltage can have a large signal swing close to rail-to-rail (from $V_{DSsat}$ to $V_{DD}$ - $V_{SDsat}$). Since the opamp is required to drive resistive load, the second stage does not have a large voltage gain. Thus, most of the gain has to be provided by the first stage. The opamp was designed based on a conventional 1.2 μm CMOS process. The simulation results for the opamp characteristics are listed in Table 4.1.

### 4.2.2 Switch problem

If a bulk-driven differential pair is used as an input stage for an opamp [45], the common-mode voltage $v_x$ can be set at $V_{DD}/2$ and analog circuits based on inverting opamp configuration such as active RC filters can be realized even at 1 V.

**Table 4.1. Simulated opamp characteristics**

| | |
|---|---|
| Supply voltage | 1V |
| Power dissipation | 0.15 mW |
| Threshold voltage | $V_{TN} \approx 0.7$ V, $V_{TP} \approx -0.8$ V |
| Unity gain bandwidth | 10 MHz |
| DC gain | 60 dB |
| Settling time (0.1 %) | 120 ns |
| Load capacitance | 20 pF |
| Load resistance | 10 kΩ |

However, analog circuits that require switches such as track-and-hold amplifiers are still not realizable using this type of opamp with $v_x$ set to $V_{DD}/2$. This is due to the fact that a voltage signal at the mid-range of the supply voltage cannot pass through the switches [47]. In general, critical switches for passing voltage signals must be avoided in low voltage design. If the proposed technique is used, NMOS switches can be added to the opamp negative input at three possible locations as shown in Figure 4.4. In this case, the switches are used to pass current signals instead of large voltage signals. For a given current, the sizes of the switches need to be determined (except for the switch $S_3$, which only affects the settling time of the circuit) to ensure that the voltage drops across the switches are minimized. If the sizes of the switches are selected appropriately, the drain voltages and the source voltages of the switches are approximately equal to $v_x$, which is only one $V_{DSsat}$ from ground. Therefore, the

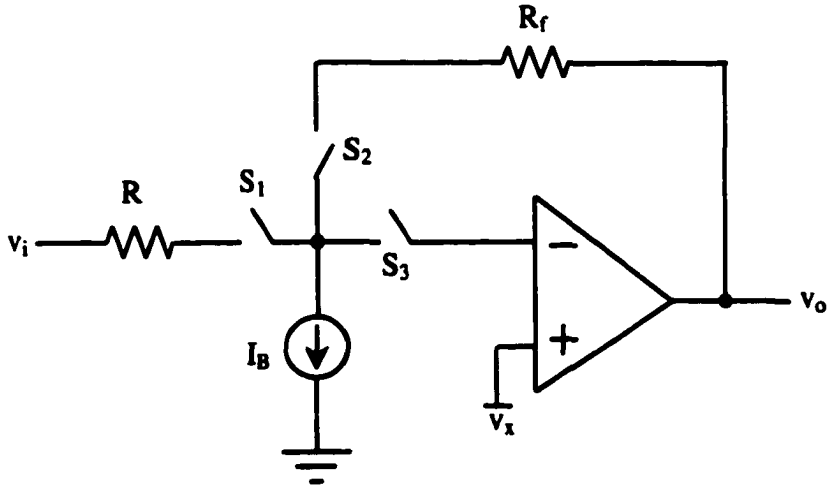



**Figure 4.4. Possible switch locations**

switches will have sufficient overdrive voltages $V_{ov}$, which is given by:

$$V_{ov} = V_{DD} - V_{tn} - v_x \qquad (4.4)$$

For a 1 V supply and $V_{tn} \approx 0.7$ V, the overdrive voltage is between 0.2 V and 0.3 V. Using these current switches, the 10-bit DAC can be realized at low supply voltage as discussed in subsection 4.2.4.

### 4.2.3 Biasing current generation

In the proposed technique, a current source or a resistor is required to allow the opamp input common mode voltage be set to $v_x$. As long as $v_x$ is generated from a reference voltage, the proposed technique that uses resistor for biasing the opamp will track with process variations as indicated in equation 4.2. However, the technique that uses current sources for biasing the opamp requires a biasing circuit for generating $I_B$ (Figure 4.5) that can track with variations on the resistor values. The resistors $R_A$ and $R_B$ are used as resistor divider to generate the opamp input common-mode voltage $v_x$ from a given fixed reference voltage $V_{ref}$. Due to the feedback loop consisting of amplifier A, $M_2$ and $R_C$, the drain voltage of $M_2$ is equal to $v_x$ and the current source $I_B$ that is used for biasing the S/H is equal to $(V_{ref} - v_x)/R_C$ where $R_C$ can be determined using equation 4.1. As a result, $I_B$ will track the variations in resistor values when the resistors are realized using the same kind of material. Notice that the drain voltages of $M_1$ and $M_2$ have the same potential equal to $v_x$, and their drain currents will be the same even if both $M_1$ and $M_2$ are in triode region. Therefore, $v_x$

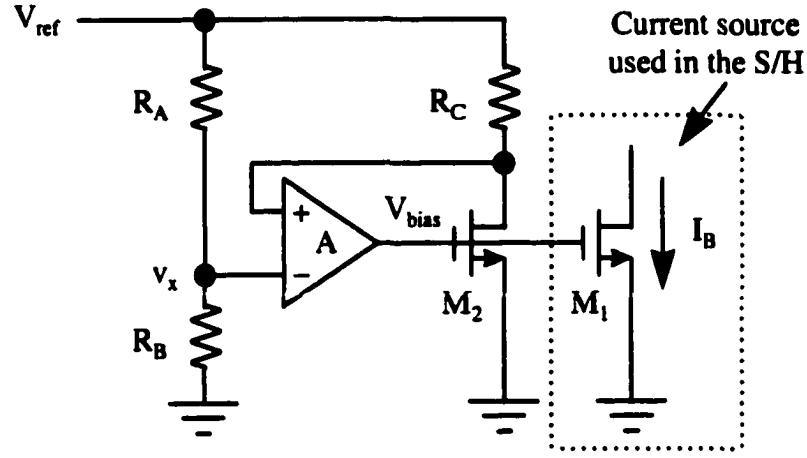



**Figure 4.5. Biasing circuit for generating $I_B$**

can be set robustly close to ground. The amplifier A can be realized as the first stage of the opamp shown in Figure 4.3.

### 4.2.4 Segmented R-2R DAC design

In the literature, different techniques have been proposed to implement DACs including the use of resistor strings, switched-capacitor techniques, current-mode approaches and R-2R techniques [20]. If current-mode approaches are to be used, a cascode current source is usually required in each DAC cell to increase the output resistance. Due to the limited area for each DAC cell in a thermometer code DAC, relatively small transistors have to be used for the cascode current sources and hence, small output signal swing will result. For other DAC techniques except R-2R techniques, voltage switches are usually required. Unless the signal swing is limited, the switches will not have sufficient overdrive voltage for low supply voltage.

Although switched-opamp techniques can be used for designing low voltage DACs, the output of the opamp has to be switched to one of the supply rails during one of the clock phases. Hence, the output of the DAC is only valid at one clock phase.

To design a low voltage DAC, a conventional R-2R DAC design can be converted into a low voltage design by applying the proposed technique discussed in the previous section. A 10-bit DAC architecture is shown in Figure 4.6. In this design, the biasing scheme that uses current source is adapted. The DAC consists of two opamps and is capable of providing fully differential outputs. Since the switches are

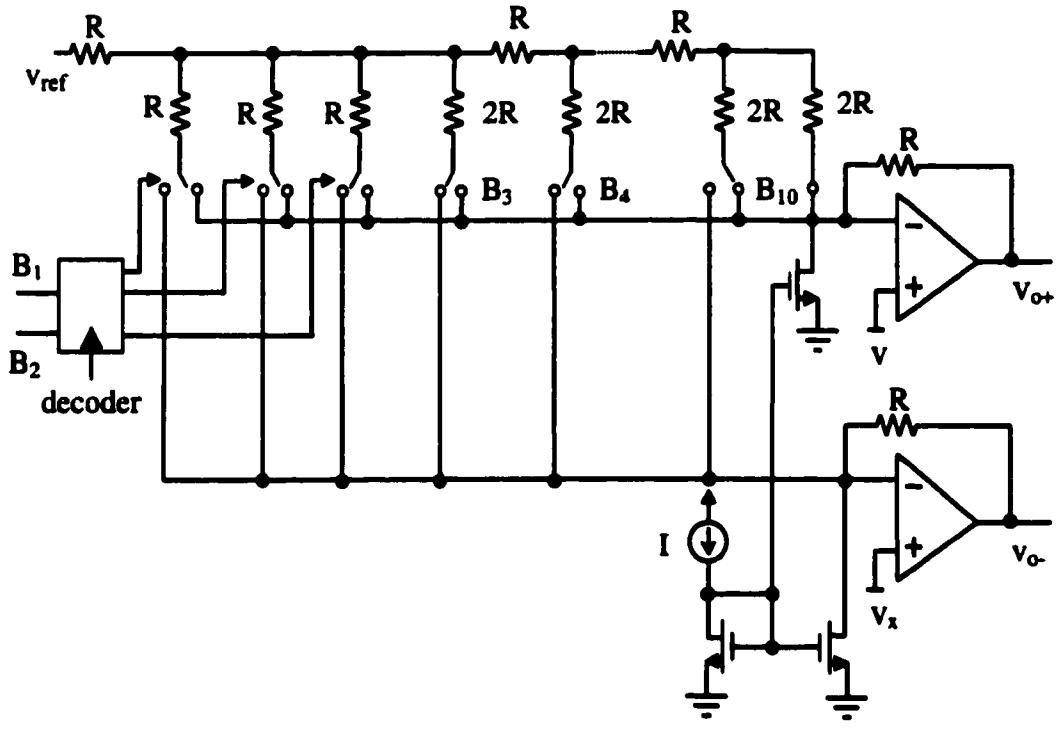



**Figure 4.6. Proposed 1V 10-bit DAC architecture**

connected between the resistors and the opamp negative input terminals, they are used for passing current signals and will have sufficient overdrive voltage as discussed before. The sizes of the switches are scaled to accommodate different resistor current levels to minimize the overall DAC nonlinearity. To relax the matching requirement of the resistors and to minimize the magnitude of glitches, the two MSB resistors are realized in one segment from three equal resistors using thermometer coding. When the input digital code is 1000000000, the positive output voltage $V_{o+}$ is desired to be at $V_{DD}/2$. For the input digital code equal to 1111111111 and 0000000000, $V_{o+}$ is desired to be close to rail-to-rail (0.9 V and 0.1 V, respectively). Based on these requirements, all resistor values can be found. $I_B$'s can be determined using equation 4.1 if $V_{ref}$, $v_x$ and $R_f$ are given. In this design, they were chosen to be 1 V, 50 mV and 20 kΩ, respectively.

### 4.2.5 Implementation and experimental results

The proposed 10-bit DAC was designed and implemented in a conventional 1.2 μm, double metal, double poly, CMOS process with $V_{tn} \approx 0.7$ V and $V_{tp} \approx -0.8$ V. The resistors were realized using polysilicon with a sheet resistance of approximately 30 Ω/square. The die photo of the DAC is shown in Figure 4.7. The DAC has an active area of 0.6 mm by 1.1 mm.

The DAC has a single-ended output swing approximately between 0.1 V and 0.9 V (close to rail-to-rail) after $V_{ref}$, $v_x$ and $I_B$ are set approximately to 1 V, 50 mV

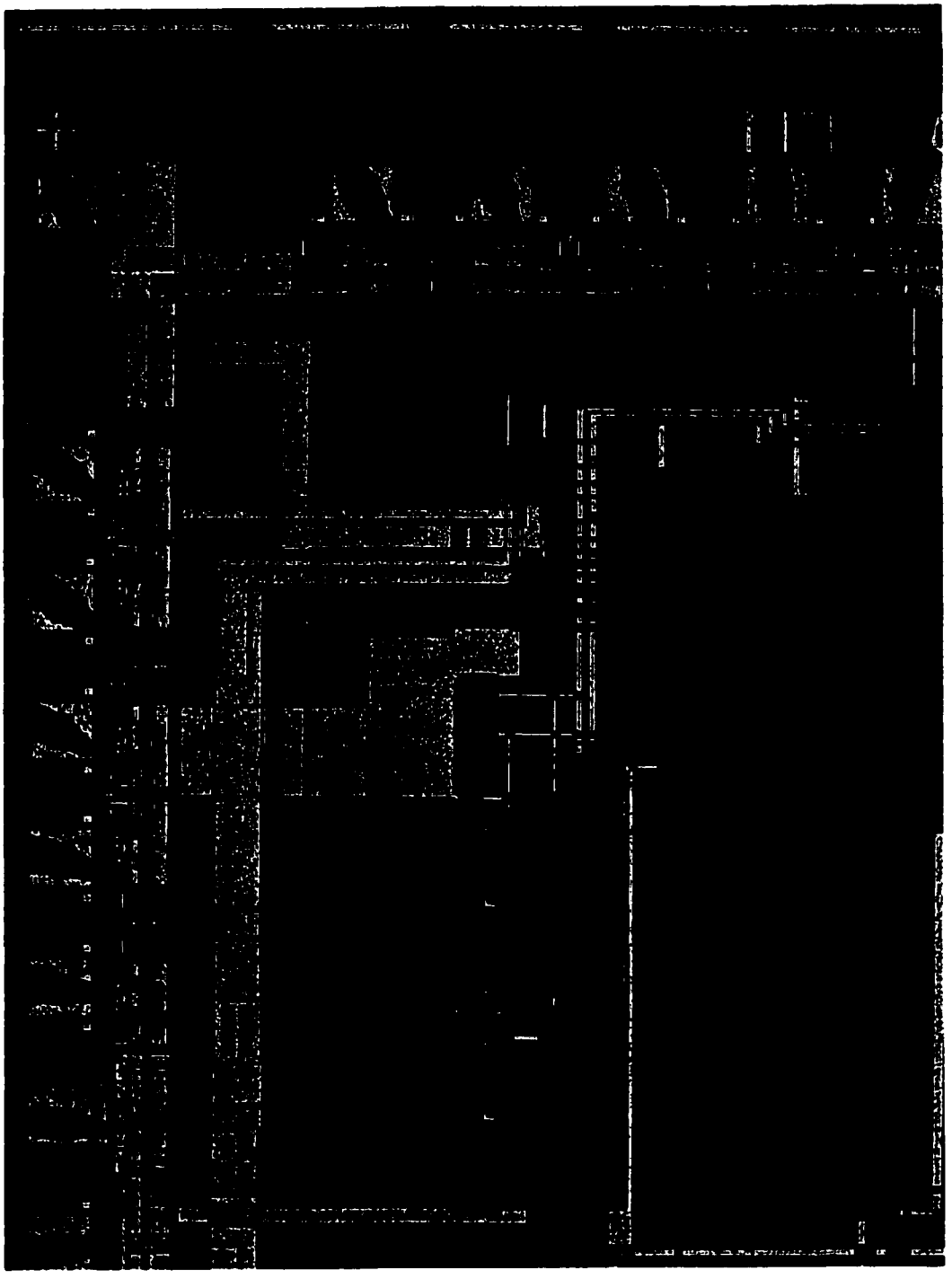


**Figure 4.7. Die photo of the 1V DAC**

and 70 μA, respectively. The total power dissipation including all the biasing currents and all the digital circuits was measured to be less than 0.45 mW at 1 V for a throughput of 1 MS/s. When the digital input was switched from its minimum value to its maximum value and vice versa, the worst case single-ended settling time with a loading capacitance of approximately 20 pF was measured and found to be less than 1 μsec as shown in Figure 4.8. The settling time for the DAC is limited by the opamp's finite gain bandwidth product and slew rate.

Similar test procedure as in subsection 2.6.1 was used for measuring the performance of the 1V DAC. DC measurement of the DAC was performed using

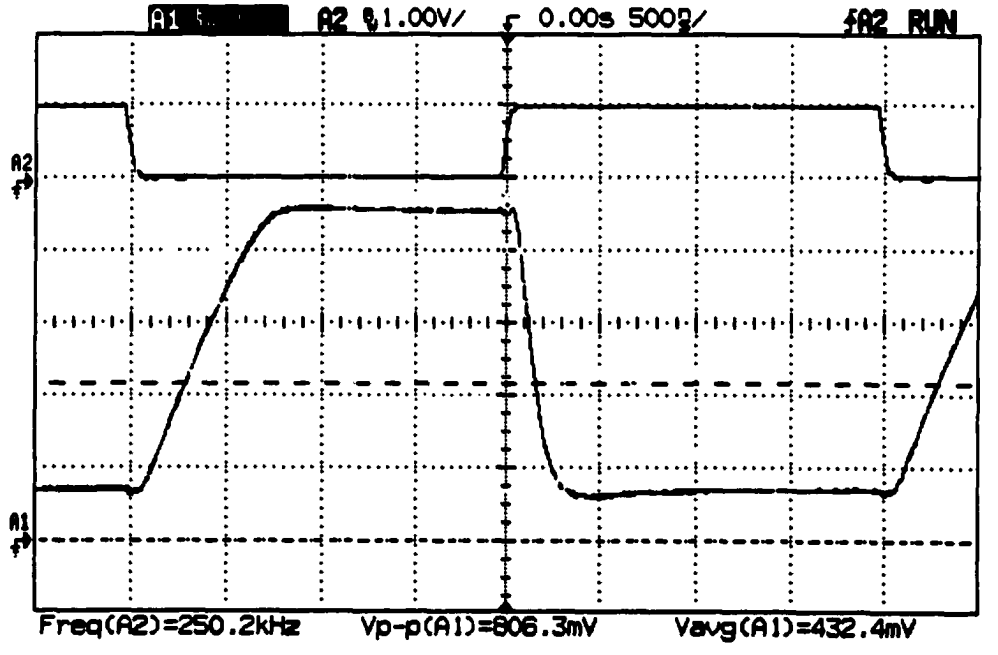



**Figure 4.8. DAC transient response (Upper: digital input values; Lower: DAC output)**

HPVEE software, a 10-bit counter, HP8904A function generator, and HP34401 digital voltmeter. HPVEE was used to control the function generator to provide a 1 Hz clock signal for the counter and the counter's 10-bit digital ramp output was applied to the input of the DAC. The DAC's analog output voltage, as read by a digital voltmeter, was saved in a file and used to measure the differential nonlinearity (DNL) and integral nonlinearity (INL) of the DAC. The DC test results are shown in Figure 4.9. The maximum DNL and INL are 1.7 LSBs and 3.0 LSBs, respectively. The nonlinearity is mainly due to the mismatch between resistors. When the supply voltage is set to 0.9 V, the DAC still operates properly with a lower output swing after proper adjustments of $V_{ref}$ and $I_B$. The performance of the 1V DAC is summarized in Table 4.2.

## 4.3 8-bit Successive Approximation ADC

In this section, the design of a 1-V, 8-bit, 50-kS/s successive approximation ADC using the above-mentioned techniques is presented. New biasing scheme and current-mode approaches are employed to design low-voltage S/H and latched comparator for the 8-bit ADC. This design demonstrates that low-voltage ADC with medium accuracy can be realized without requiring special enhancements to CMOS technology. The block diagram of the successive approximation ADC is shown in Figure 4.10. Besides the successive approximation register and control logic, the ADC consists of three major analog building blocks — a sample-and-hold circuit

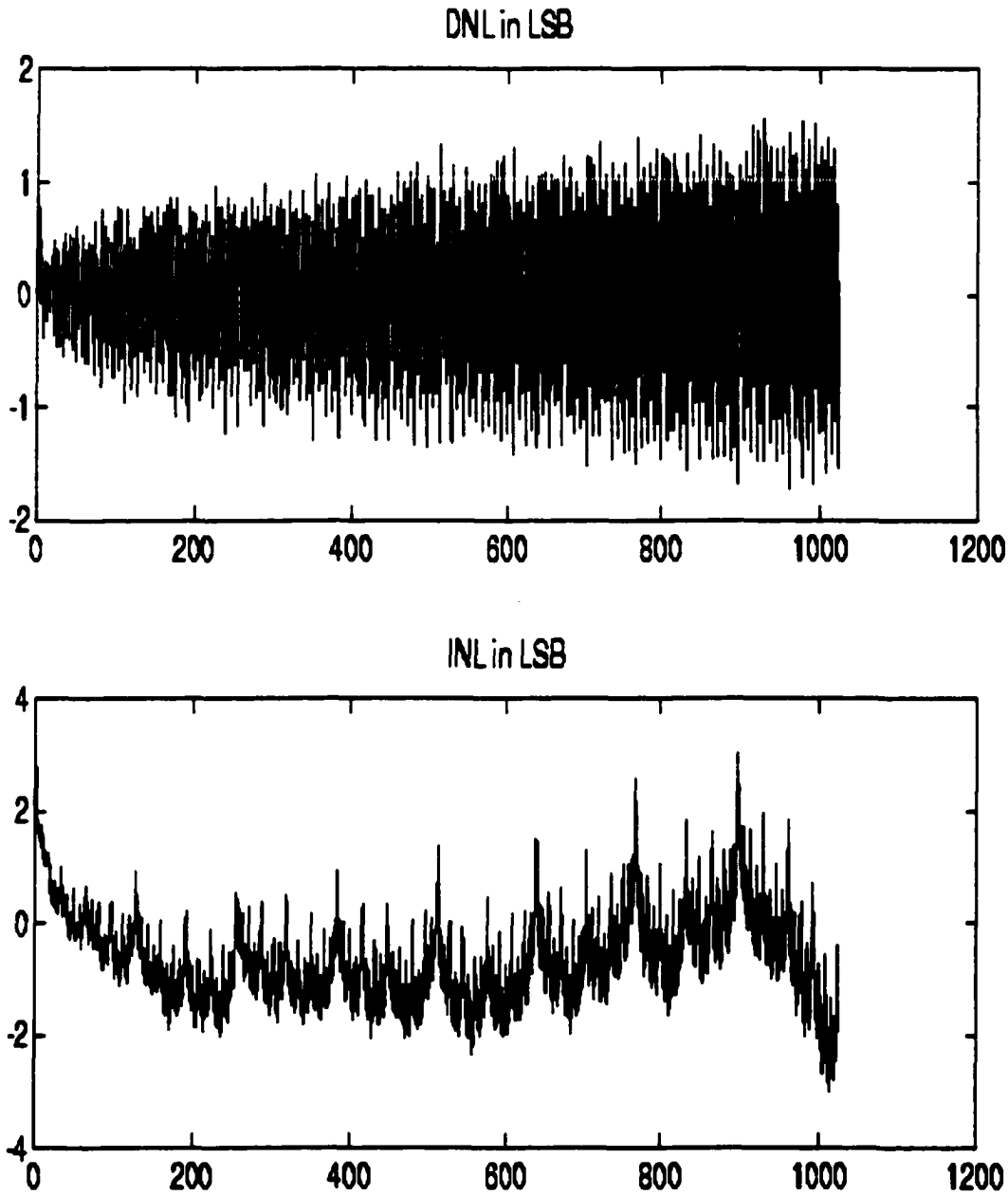



**Figure 4.9. Measured DNL and INL for the 1V DAC**

**Table 4.2. Measured performance of the 1V DAC**

| | |
|---|---|
| Supply voltage | 1 V |
| Power dissipation | 0.45 mW |
| Technology | 1.2 μm CMOS<br>($V_{TN} \approx 0.7$ V, $V_{TP} \approx -0.8$ V) |
| Throughput | 1 MS/s |
| Resolution | 10 bits |
| DNL | 1.7 LSB |
| INL | 3.0 LSB |
| Active area | 0.6 mm by 1.1 mm |
| Output swing | 800 mV |

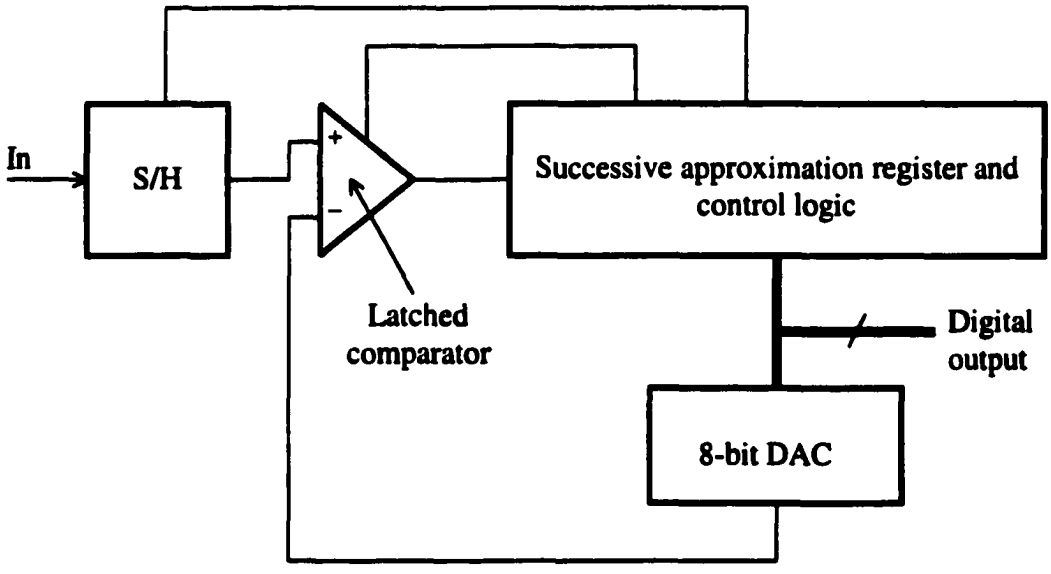



**Figure 4.10. Block diagram of the successive approximation ADC**

(S/H), an 8-bit digital-to-analog converter (DAC) and a latched comparator. The DAC has similar structure as discussed in section 4.1. The S/H and comparator will be discussed in subsections 4.3.1 and 4.3.2, respectively. The measured results are summarized in subsection 4.3.3.

### 4.3.1 Sample-and-Hold design

Most of sample-and-hold (S/H) designs in CMOS technology are based on switched-capacitor techniques. A typical design is shown in Figure 4.11. When this S/H is operated at low voltage (for example, 1 V), the input and output must have large signal swing to maximize the signal-to-noise ratio. Since the threshold voltages for NMOS and PMOS in a conventional CMOS process are in the range of 0.5 V to 0.9 V, the switches will fail to pass voltage signals in the mid range of the supply rails even if transmission gates are used [47].

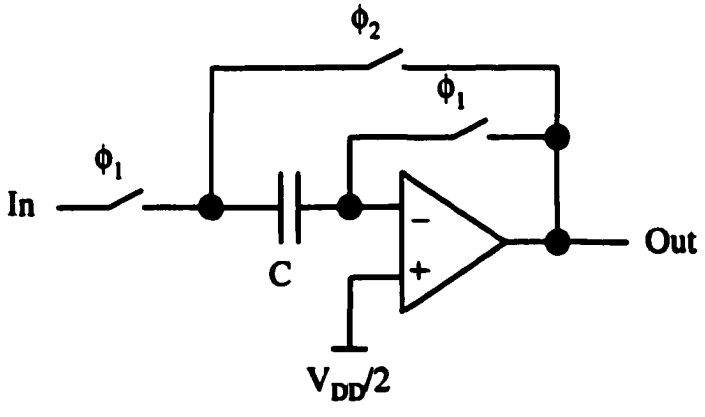



**Figure 4.11. Typical CMOS S/H**

To design a S/H that can operate at 1 V, a S/H similar to the traditional design of Figure 4.12 that uses resistors is developed. This S/H amplifier is shown in Figure 4.13. The opamp is the same as the one used in the DAC. When $\phi_1$ turns high, the S/H is in sampling mode and is configured as an inverting amplifier with a gain of $-R_2/R_1$. The holding capacitor C acts as a capacitive load to the opamp. The opamp output is sampled by the holding capacitor at the falling edge of $\phi_1$. Since the input and output of the S/H are connected to resistors, the signal swing can be close to the supply rails. The input common-mode voltage of the S/H is set at $v_x$, which is about one $V_{DSsat}$ above the ground voltage to ensure sufficient drain-to-source voltage for M1 to operate as a current source. Using this current source, the input and output quiescent voltages can be set at $V_{DD}/2$. The required current $I_1$ can be determined using the following expression:

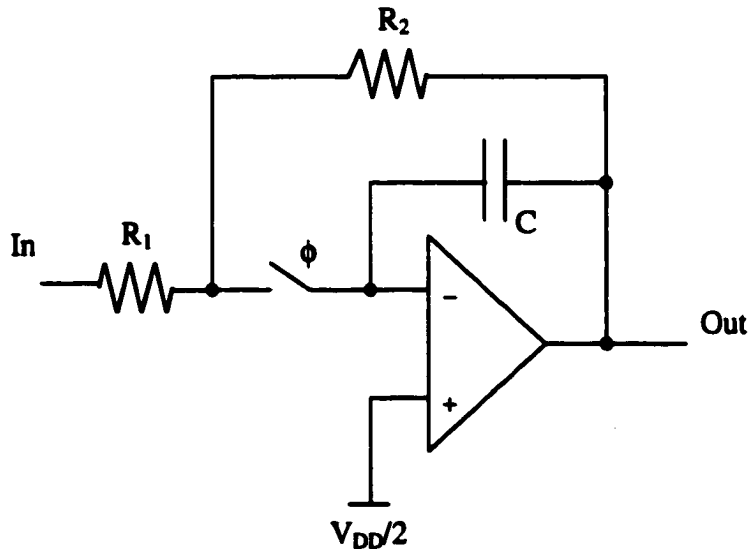



**Figure 4.12. Traditional S/H using resistors**

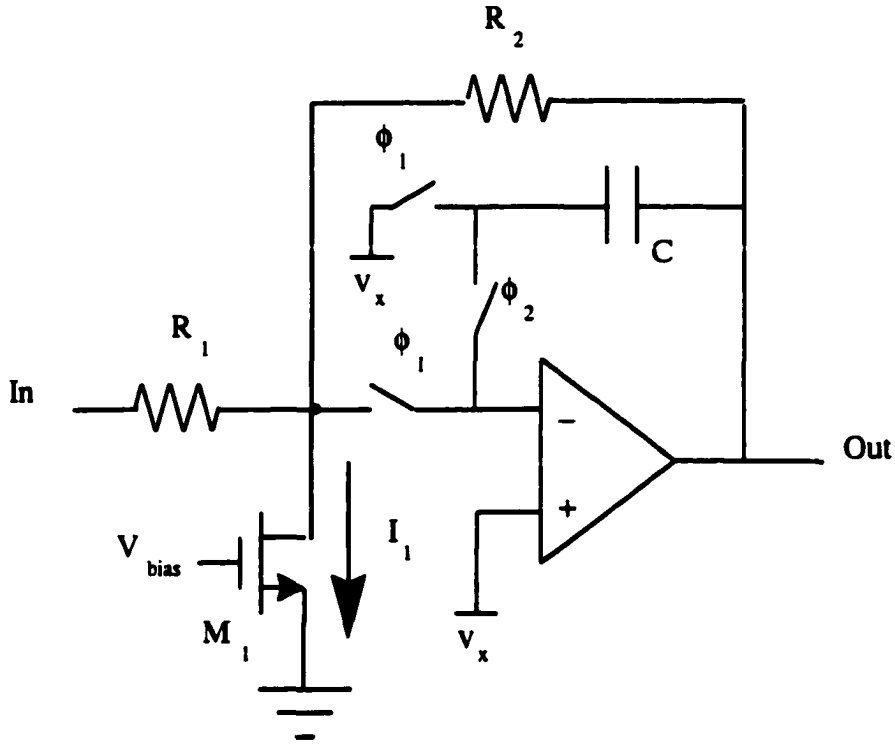



**Figure 4.13. Low-voltage S/H**

$$I_1 = \left(\frac{V_{DD}}{2} - v_x\right)\left(\frac{1}{R_2} + \frac{1}{R_1}\right) \qquad (4.5)$$

When $\phi_2$ turns high, the S/H is in hold mode, and the holding capacitor C is connected between the negative input and the output of the opamp.

Since the switches used in the S/H are only required to pass current signals, they can be realized using NMOS transistors. It can be observed that the switches will have sufficient overdrive voltage, which is equal to $V_{DD}$ - $V_{TN}$ - $v_x$. The minimum required $V_{DD}$ is equal to the maximum input common-mode of the opamp plus the

$V_{DSsat}$ of $M_1$ and is approximately equal to $|V_T| + 3V_{DSsat}$. Without the current source $I_1$, the minimum required $V_{DD}$ is approximately given by $2|V_T| + 4V_{DSsat}$. Nonlinearity errors of the S/H due to charge injection of the switches are minimized since the drain and source voltages of the switches are always connected to the same potential $v_x$. However, clock feedthrough due to the switches will produce an offset voltage at the input of the S/H and hence, affect the overall offset error of the ADC. In some applications, this offset error may not be of major concern.

For the traditional S/H shown in Figure 4.12, the holding capacitor C is always connected in parallel with the feedback resistor $R_2$. In this case, the -3 dB bandwidth during sampling mode is approximately given by $1/R_2C$. A high bandwidth is usually desired to minimize the tracking error. For the S/H shown in Figure 4.13, the holding capacitor C appears as a load capacitance to the opamp during the sampling mode. Therefore, the -3 dB bandwidth of the S/H is equal to $\omega_T/[1 + R_2/(R_1//r_{ds1})]$ where $\omega_T$ is the unity gain bandwidth of the opamp. Therefore, the S/H shown in Figure 4.13 will have higher bandwidth than the traditional S/H. Since the -3 dB bandwidth is dependent on $\omega_T$ and is almost independent of the holding capacitor C, the S/H will have less tracking error.

To design the S/H that can track with process variation, the current source used for biasing the S/H must track with variations in resistor values. As explained in subsection 4.1.3, this can be achieved using the biasing circuit shown in Figure 4.5.

### 4.3.2 Latched comparator design

The S/H and the DAC discussed in the previous sections are designed to have large voltage swing to maximize the dynamic range. As a result, the latched comparator used in the ADC must have an input common-mode range close to rail-to-rail. Conventionally, voltage comparators are designed with a differential pair as the input stage. Unfortunately, the input common-mode range is limited for 1 V operation. Furthermore, using switched-capacitor techniques to shift the input voltages to an acceptable input common-mode range before comparison may not be possible since switches cannot be used for passing voltage signals in the mid range of the supply rails. Although rail-to-rail differential input stages have been reported [42] [44], it is still difficult to achieve 1 V operation in a standard CMOS process.

To design a low-voltage latched comparator with wide input swing, a current-mode approach is employed as shown in Figure 4.14. Nodes A and B have very low input impedance and can be determined as $1/g_{m1}g_{m2}r_{ds3}$. The quiescent voltage $V_Q$ for both nodes is approximately equal to $V_{DD} - V_{GS2}$. Therefore, the currents $i_1$ and $i_2$ flowing to nodes A and B are equal to $[V_A + V_B - 2V_Q]/2R$ and $(V_{DD}/2 - V_Q)/R$, respectively where $V_A$ is connected to the S/H output, and $V_B$ is connected to the negative DAC output. Effectively, $i_1$ is proportional to the voltage difference between the S/H output and the DAC output plus a quiescent current of $(V_{DD}/2 - V_Q)/R$. This quiescent current is due to the voltage difference between the quiescent output voltages of the S/H and the DAC and the quiescent voltage of node A. Current $i_2$ is

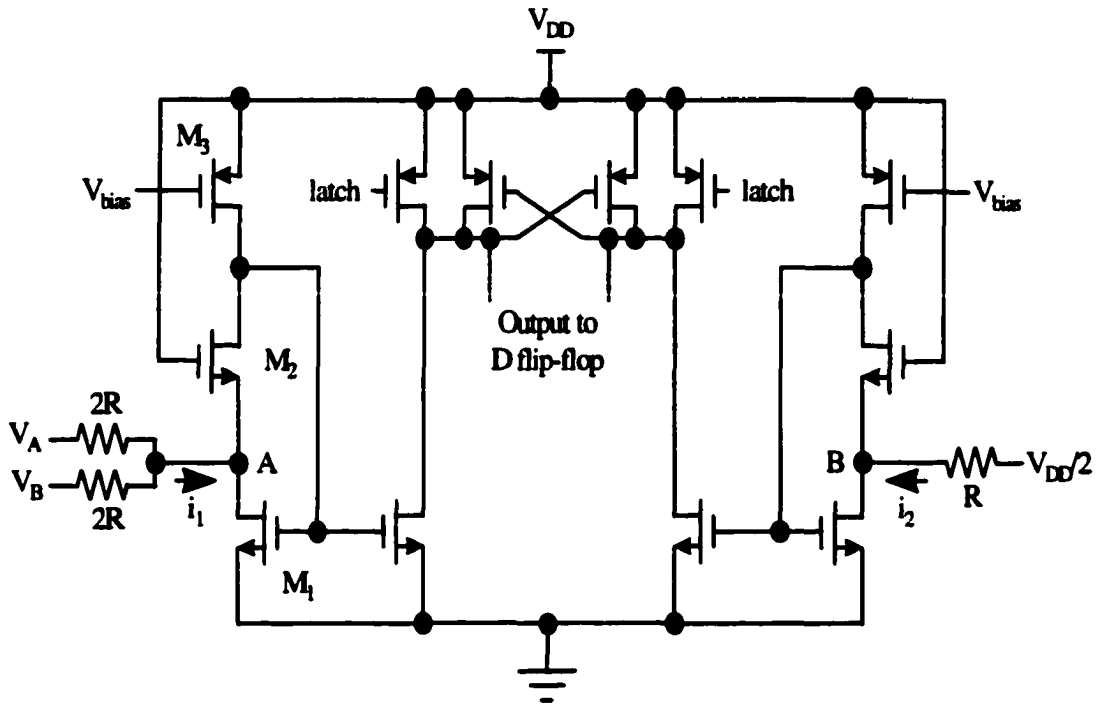



**Figure 4.14. Low-voltage latched comparator using current-mode approach**

used for generating a reference current for comparison. When the latch signal turns high, $i_1$ and $i_2$ are compared, and a digital signal is generated at the output nodes. Since the comparator inputs are connected to resistors, high input signal swings can be obtained. The minimum supply voltage required for proper operation of the comparator is given by $\max\{V_{TN2} + V_{DSsat2} + V_{DSsat1}, V_{SDsat3} + V_{DSsat2} + V_{DSsat1}\}$, which is usually lower than 1 V. The offset of the comparator depends on the mismatches between the MOSFETs and also the mismatches between the resistors. However, this offset will only affect the overall offset of the ADC but not the overall linearity.

### 4.3.3 Implementation and experimental results

The 8-bit successive approximation ADC was designed and fabricated in a conventional, low-cost 1.2 μm CMOS process with $V_{TN} \approx 0.7$ V and $|V_{TP}| \approx 0.8$ V. The die photo is shown in Figure 4.15. The ADC has an active area of about 1.8 mm by 1.8 mm. All the resistors had values between 20 kΩ and 40 kΩ, and were realized using polysilicon with a sheet resistance of about 30 Ω/square. The holding capacitor in the S/H had a value approximately equal to 1.5 pF. To simplify the design of the ADC, the biasing circuit of Figure 4.5 was omitted in the actual implementation. Instead, external resistors were used for generating the required biasing currents. The total power dissipation including all the biasing currents, the digital control logic, and the digital pads was measured to be less than 0.34 mW for a sampling rate of 50 kS/s and a supply voltage of 1 V. Each opamp dissipates approximately 90 μW.

To facilitate the performance measurement of the DAC, the successive approximation ADC was designed to allow digital input signals to control the DAC inputs directly. The DAC was capable of operating at a sampling rate of over 500 kS/s with an output swing between 0.075 V and 0.925 V.

A separated S/H that had the same structure as the one shown in Figure 4.13 was also fabricated on a different chip. The measured S/H characteristics are listed in Table 4.3. The entire ADC was tested at a sampling rate of 50 kS/s. Similar test procedure as in subsection 2.6.2 was used for testing the 1V ADC.

Code density measurement was used to measure the DNL and INL of the

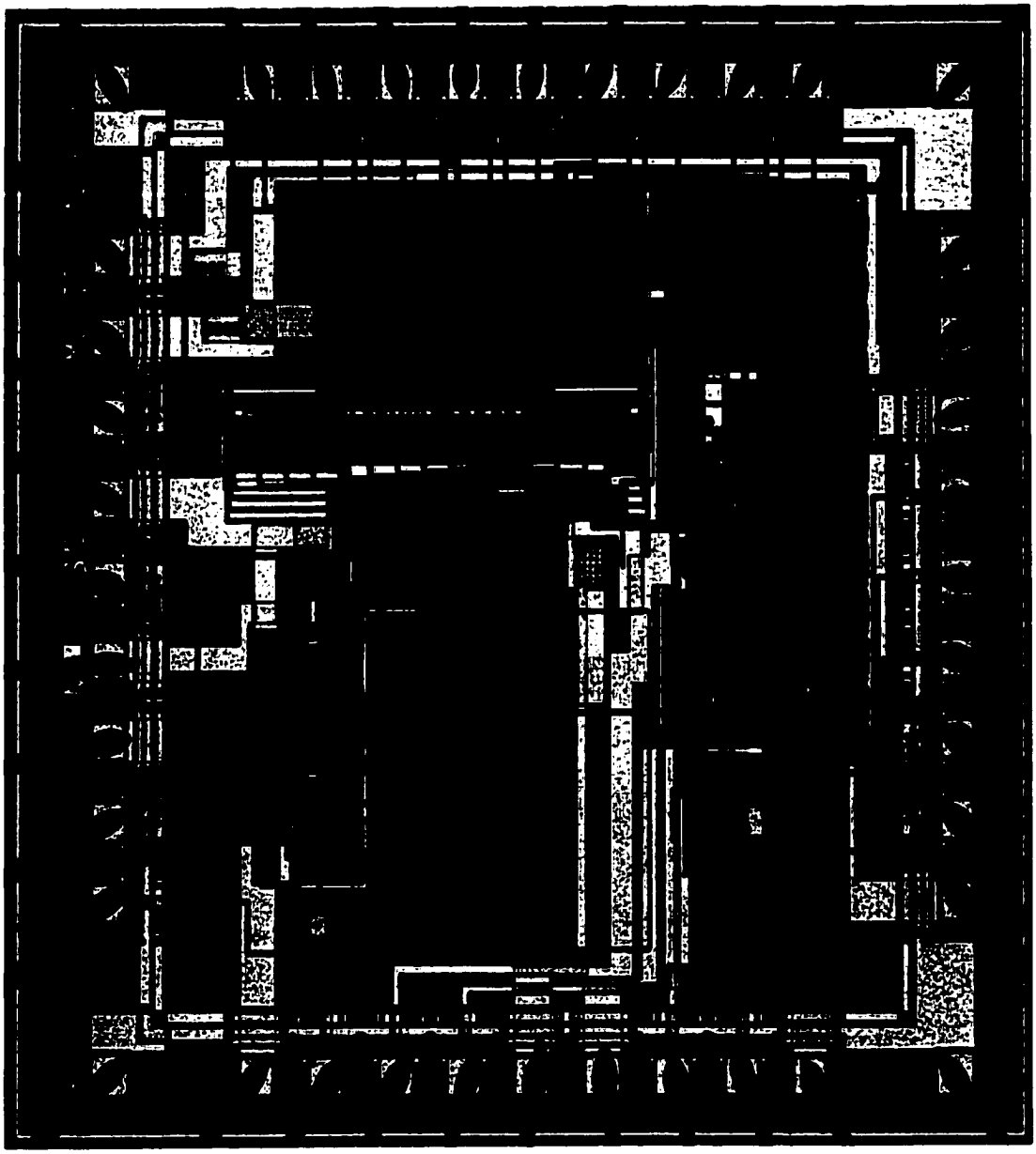


**Figure 4.15. Die photo of the 1V ADC**

**Table 4.3. Measured performance of the 1V S/H**

| | |
|---|---|
| Supply voltage | 1 V |
| Sampling rate | 500 kS/s |
| Input Frequency | 50 kHz |
| Track mode distortion | -70 dB |
| Track-and-hold mode distortion | -62 dB |
| Output swing | 0.1 - 0.9 V |

ADC. First, a very low frequency (0.1 Hz) ramp signal with 1V peak-to-peak amplitude (slightly larger than the maximum input range of the ADC) was applied to the input of the ADC. Then the digital output of the ADC was recorded using a Tektronix TLA711 logic analyzer. The digital code was used to measure the DNL and INL of the ADC. The DC test results are shown in Figure 4.16. The maximum values of DNL and INL are 0.47 and 1.41 LSB, respectively.

For AC test of the ADC, a 1 kHz, 850 mV peak-to-peak input signal was applied to the input of our ADC at a sampling rate of 50 kS/s. The 8 output bits of our ADC were applied to a 1V to 5V level shifter. The level shifter was built using CMOS inverters and resistive voltage dividers. The outputs of the level shifter were then applied to the 8 MSB inputs of a 12-bit commercial DAC with part number MAX507. Figure 4.17 shows the output of the MAX507 as measured by a Tektronix 2710 spectrum analyzer. The output spectrum was used to calculate the SFDR,

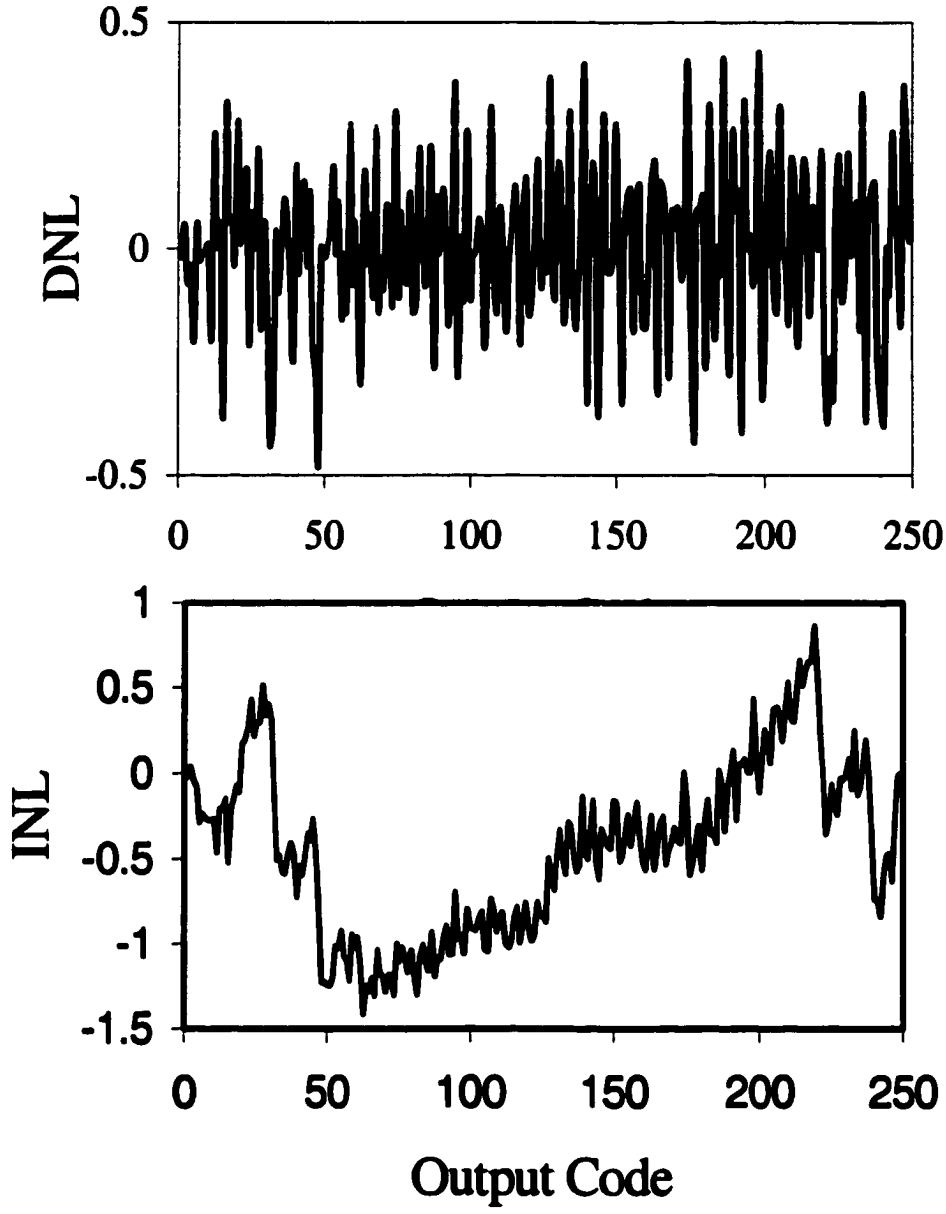



**Figure 4.16. DNL and INL of the 1V ADC (in LSB)**

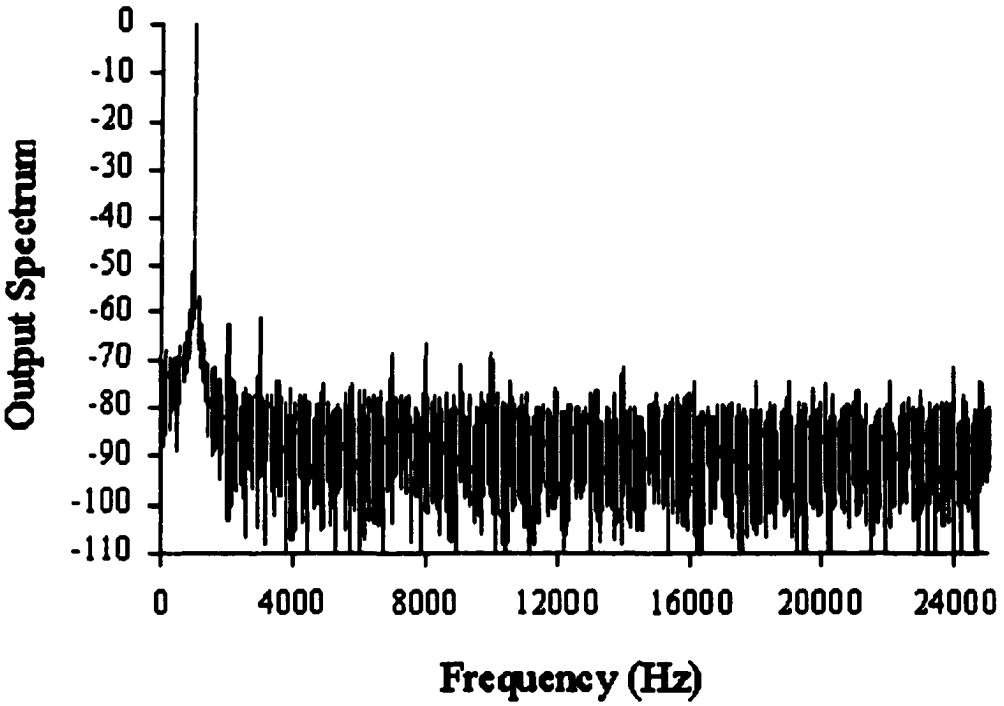



**Figure 4.17. Output spectrum of the 1V ADC for a 1 kHz input**

SNDR, and ENOB of our ADC. In these measurements, we assumed that MAX507 is an ideal DAC and all the nonlinearity and noise are due to our ADC. The measured ENOB of our ADC is 7.9 bits at a sampling rate of 50 kS/s. The ENOB vs. input frequency is shown in Figure 4.18. For low input frequencies, the ENOB is close to the ideal case. The ENOB drops to 7.0 bits at 8 kHz. This degradation is mainly due to the degradation in the performance of the DAC for high input frequencies. The performance of the 8-bit ADC is summarized in Table 4.4.

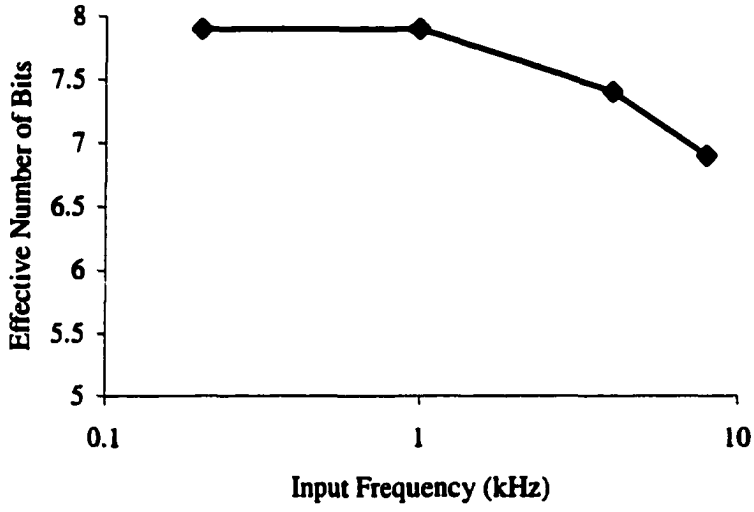



**Figure 4.18. ENOB vs. input frequency for the 1V ADC**

**Table 4.4. Measured performance of the 1V ADC**

| | |
|---|---|
| Supply voltage | 1 V |
| Power dissipation | 0.34 mW |
| Technology | 1.2 μm CMOS<br>($V_{TN} \approx 0.7$ V, $V_{TP} \approx -0.8$ V) |
| Sampling rate | 50 kS/s |
| Resolution | 8 bits |
| Active area | 1.8mm × 1.8 mm |
| Input swing | 850 mV |
| DNL | 0.47 LSB |
| INL | 1.41 LSB |
| ENOB @ 1 kHz | 7.9 bits |

## 4.4 Summary

A technique for converting analog circuits that utilize inverting opamp configurations into low voltage designs is proposed. To minimize the supply voltage, a current source or a resistor is introduced between the opamp negative input terminal and one of the supply rails such that the opamp input common-mode voltage can be biased close to one of the supply rails, independent of the quiescent input and output voltages. Based on this technique, an opamp with limited input common-mode range can be used for low voltage design. Furthermore, low voltage analog circuits such as low voltage continuous time active RC filters can be realized without the need for a specialized process or using bulk driven MOSFETs. The minimum supply voltage for the proposed technique is approximately equal to $3V_{DSsat} + V_T$. For analog circuits that require switches, switches for passing current signals can be incorporated into the proposed technique by placing the switches at the opamp negative input terminal. At this location, the switches will have sufficient overdrive voltages. Therefore, critical voltage switches can be avoided. It should be mentioned that although the proposed technique can be applied to design many useful low voltage analog circuits, it cannot be used directly to replace switched-opamp or switched-capacitor class of circuits since some circuits may be more effectively realized using the later techniques.

To demonstrate the proposed technique, a 10-bit DAC was designed and implemented in a conventional 1.2 μm CMOS process. The design is capable of operating at a very low voltage (1 V) with low power consumption (< 0.45 mW) with

a wide input and output signal swing close to rail-to-rail. From the experimental results, the DAC has a maximum DNL of 1.7 LSBs, a maximum INL of 3.0 LSBs and a throughput of 1 MS/s for an output swing between 0.1 V and 0.9 V.

Using the same techniques, a 1V, 8-bit, 50-kS/s successive approximation ADC was also presented and implemented in a standard, low-cost 1.2 μm CMOS process. New biasing scheme and current-mode approaches have been employed to design low-voltage S/H and latched comparator for the 8-bit ADC. The ADC was measured to have a power dissipation of less than 0.34 mW for a 1V supply and an ENOB of 7.9 bits for 1 kHz input with close to rail-to-rail signal swing. This design demonstrates that low-voltage ADC with medium accuracy can be realized without requiring special enhancements to CMOS technology. The ADC is designed for medium quality voice and audio applications.

# CHAPTER 5. CONCLUSION AND CONTRIBUTIONS

## 5.1 Conclusion

In this dissertation, we addressed the issues of integration and programmability in reducing the power dissipation in data converters. We also developed several techniques at both architecture and circuit design levels to minimize power dissipation in some data converters for specific applications. Several prototype chips were designed and fabricated in different CMOS processes to test the performance of the proposed architectures and verify their effectiveness in terms of power savings.

## 5.2 Contributions

In chapter 2 we presented a programmable data converter cell (PDCC) which can be programmed to operate as a divide by two ($x2^{-1}$), multiply by two (x2), or sample and hold ( S/H ). The cell was used as a building block in a reconfigurable data converter (RDC). We also proposed a converter-test architecture using RDC, which is much more flexible than fixed data converters for testing analog circuits. Furthermore, it can be combined with FPGAs to create a mixed signal field

programmable array for rapid prototyping of mixed signal circuits. A prototype RDC was fabricated and its test results were presented.

In chapter 3 a design technique that uses nonlinear digital-to-analog converter (DAC) for implementing low-power direct digital frequency synthesizer (DDFS) is proposed. The nonlinear DAC is used in place of the ROM lookup table for phase-to-sine amplitude conversion and the linear DAC in a conventional DDFS. Since the proposed design technique for DDFS does not require a ROM, significant saving in power dissipation is resulted. The design procedure for implementing the nonlinear DAC is presented. To demonstrate the proposed technique, two quadrature DDFSs one using nonlinear resistor string DACs and the other using nonlinear current-mode DACs were implemented. At 3.3 V supply, the resulted power dissipations for two DDFSs are 4 mW and 92 mW at clock rates of 25 MHz and 230 MHz, respectively. For both DDFSs, the spurious free dynamic ranges were measured to be over 55 dBc for low synthesized frequencies.

In chapter 4 simple but effective biasing techniques to convert inverting opamp circuits to low voltage designs is proposed. Based on these techniques, a prototype low-voltage and low-power 10-bit segmented R-2R DAC and an 8-bit successive approximation ADC were designed and tested in a conventional 1.2 μm CMOS process.

The results of this research work have been presented in the following professional conference and journals. In September 1998, the low-power DDFS

design using nonlinear resistor string DAC was presented in the Proceedings of the 24th European Solid-State Circuits Conference [3]. The results of both DDFS designs, as discussed in chapter 3, were also published in the October 1999 issue of IEEE Journal of Solid-State Circuits [4]. The results of the low voltage 10-bit DAC design were presented in an article that was published in the March 2000 issue of IEEE Transaction on Circuits and Systems II: Analog and Digital Signal Processing [5]. Also, the low-voltage 8-bit ADC design was published in the April 2000 issue of IEEE Journal of Solid-State Circuits [6].

## 5.3 Recommended Future Work

In the pipelined reconfigurable data converter, digital self-calibration technique can be implemented using an FPGA or a digital signal processor to improve the linearity.

In the DDFS designs, digital ROM compression techniques can be applied to the non-linear DACs to further reduce the area and power. Also the current cell in the current steering non-linear DAC can be improved. The proposed technique can also be extended to design other types of non-linear DAC such as switched capacitor.

The biased inverting opamp technique can be used in designing many other low-voltage, low-power analog circuits that use inverting opamps.

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